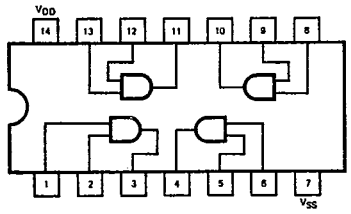
GD4081B

QUAD 2-INPUT AND GATE

DESCRIPTION — The 4081B is a positive logic Quad 2-Input AND Gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V			LIMITS V_{DD} = 10 V			LIMITS V_{DD} = 15 V			UNITS	TEMP	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	µA	MIN, 25°C	All inputs at 0V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

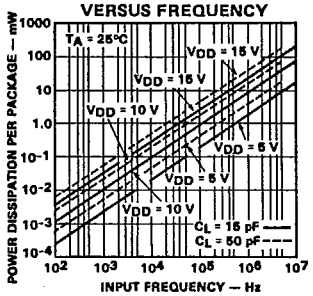
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V			LIMITS V_{DD} = 10 V			LIMITS V_{DD} = 15 V			UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		55	95		23	50		17	40	ns	C_L = 50 pF,
t_{PHL}			60	95		25	50		19	40	ns	R_L = 200 kΩ
t_{TLH}	Output Transition		70	135		30	70		23	45	ns	Input Transiton
t_{THL}	Time		57	135		23	70		16	45	ns	Times ≤ 20 ns

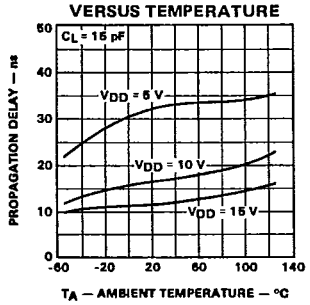
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE