

# HD74LS193

## Synchronous Up / Down Binary Counter (dual clock lines)

REJ03D0455-0200

Rev.2.00

Feb.18.2005

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the output change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes, which are normally associated with asynchronous (ripple clock) counters. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high. This counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load inputs is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words. This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions.

The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count up input when an overflow condition exists.

The counters can be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

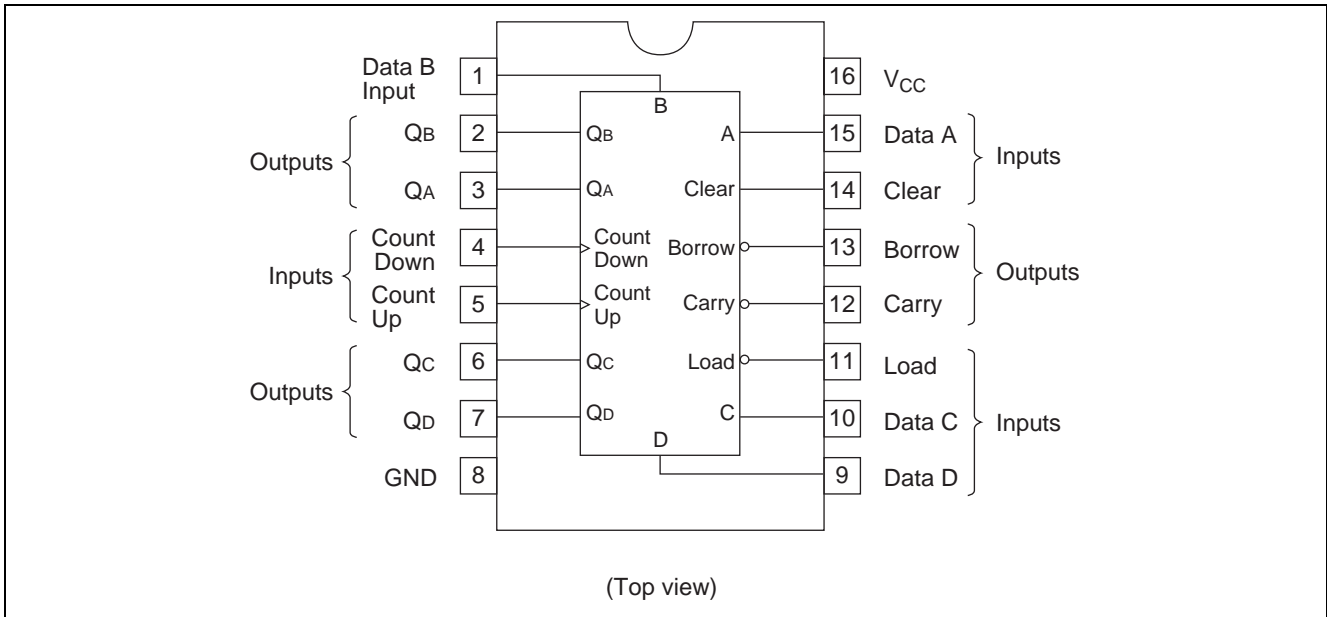
### Features

- Ordering Information

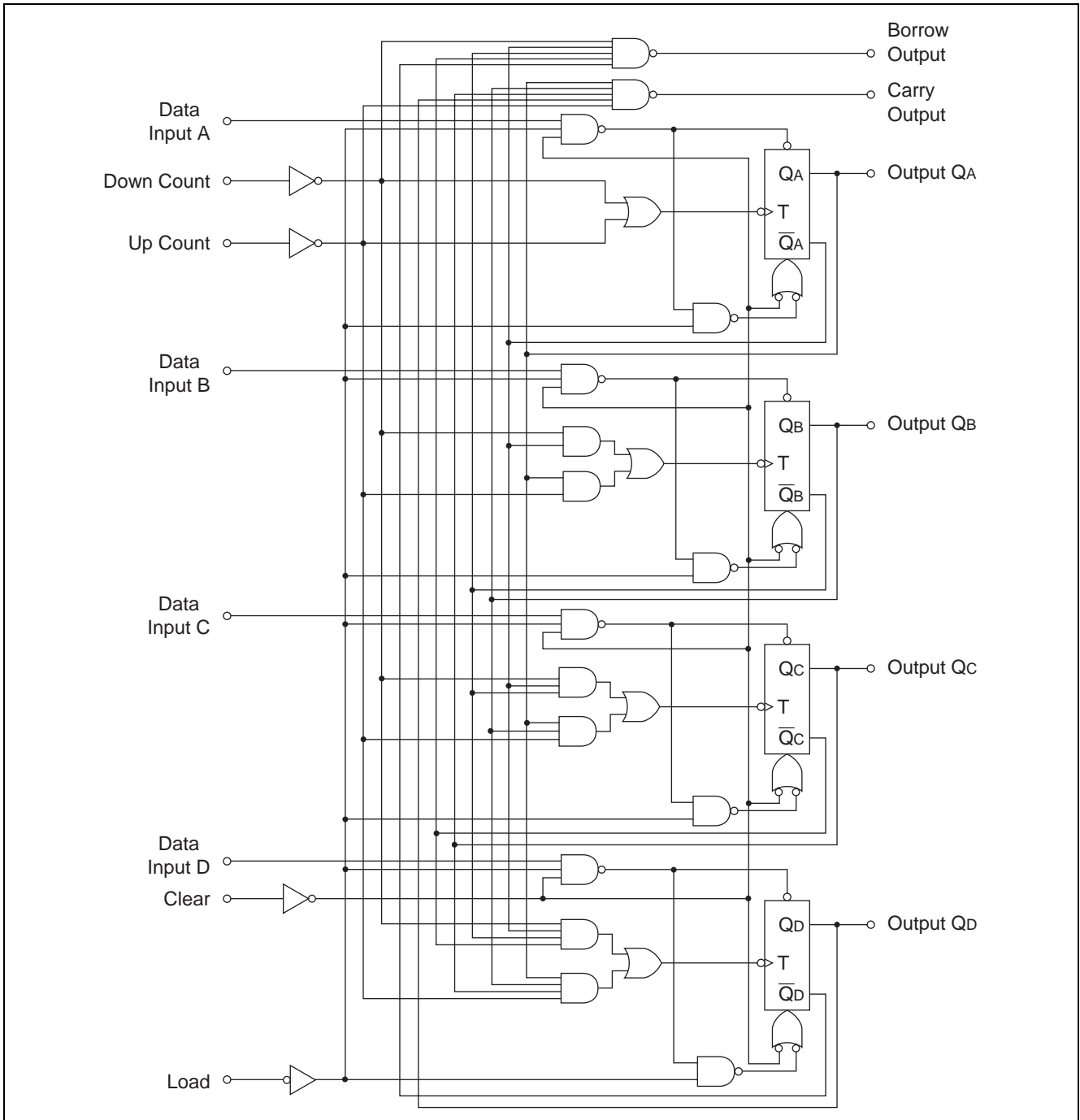
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS193P DILP-16	16 pin	PRDP0016AE-B (DP-16FV)	P —	
HD74LS193FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS193RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7 V	
Input voltage	$V_{IN}$	7 V	
Power dissipation	$P_T$	400 mW	
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

### Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75 5.00 5.25			V
Output current	$I_{OH}$	— —		-400	$\mu A$
	$I_{OL}$	— —		8	mA
Operating temperature	$T_{opr}$	-20 25		75	$^{\circ}C$
Clock frequency	$f_{clock}$	0 —		25	MHz
Pulse width	$t_w$	20 —		—	ns
Setup time (Clear)	$t_{su (CLR)}$	40 —		—	ns
Setup time	$t_{su}$	20 —		—	ns
Hold time	$t_h$	3 —		—	ns

### Electrical Characteristics

( $T_a = -20$  to  $+75^{\circ}C$ )

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	$V_{IH}$ 2.0		—	—	V	
	$V_{IL}$ —		—	0.8	V	
Output voltage	$V_{OH}$ 2.7		—	—	V	$V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -400 \mu A$
	$V_{OL}$	— —		0.4	V	$I_{OL} = 4 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V$
		— —		0.5	$I_{OL} = 8 mA$	
Input current	$I_{IH}$ —		—	20	$\mu A$ V	$V_{CC} = 5.25 V, V_I = 2.7 V$
	$I_{IL}$ —		—	-0.4	mA	$V_{CC} = 5.25 V, V_I = 0.4 V$
	$I_I$ —		—	0.1	mA	$V_{CC} = 5.25 V, V_I = 7 V$
Short-circuit output current	$I_{OS}$ -20		—	-100	mA	$V_{CC} = 5.25 V$
Supply current**	$I_{CC}$ —		19	34	mA	$V_{CC} = 5.25 V$
Input clamp voltage	$V_{IK}$ —		—	-1.5	V	$V_{CC} = 4.75 V, I_{IN} = -18 mA$

Notes: \*  $V_{CC} = 5 V, T_a = 25^{\circ}C$

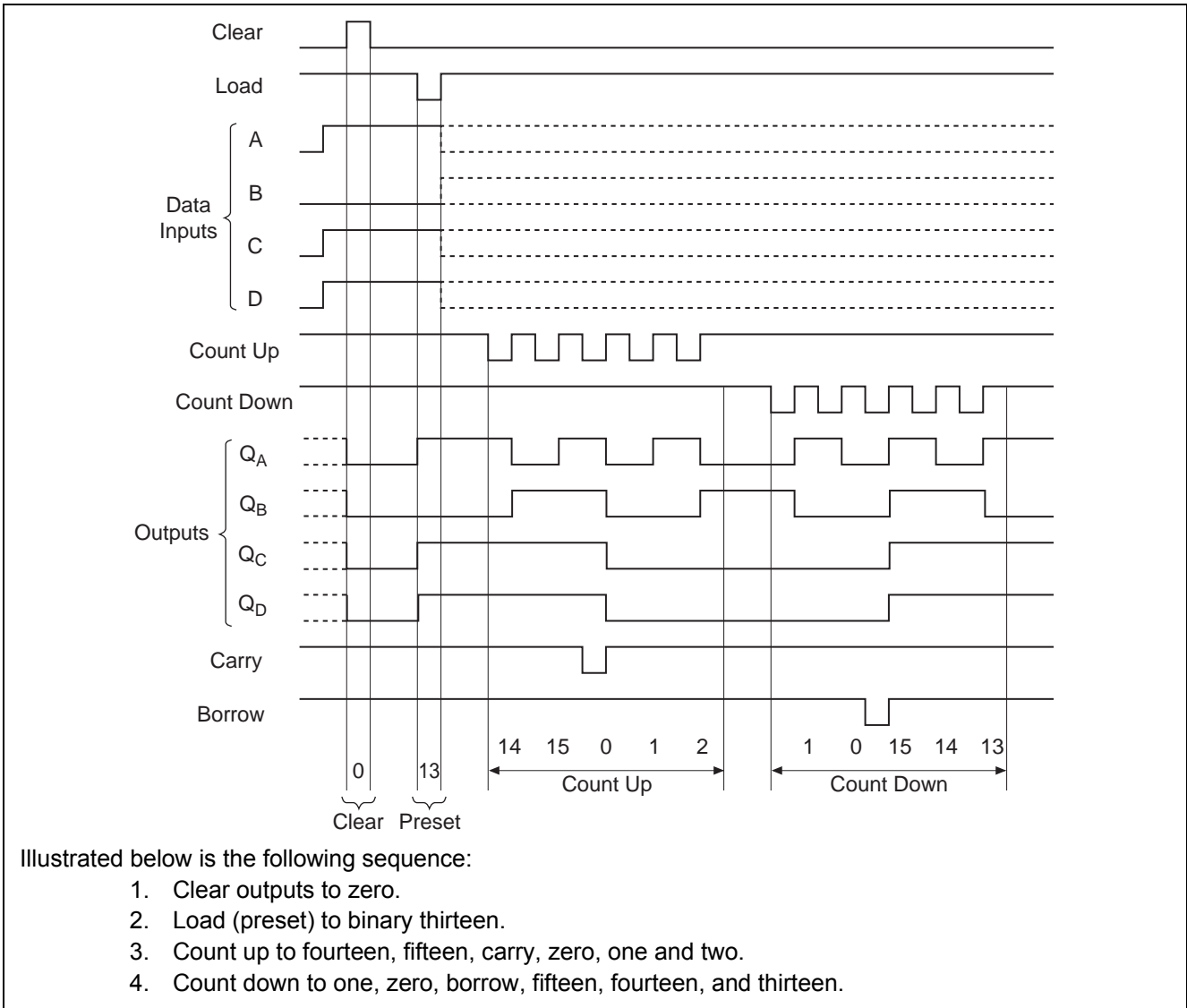
\*\*  $I_{CC}$  is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

### Switching Characteristics

( $V_{CC} = 5 V, T_a = 25^{\circ}C$ )

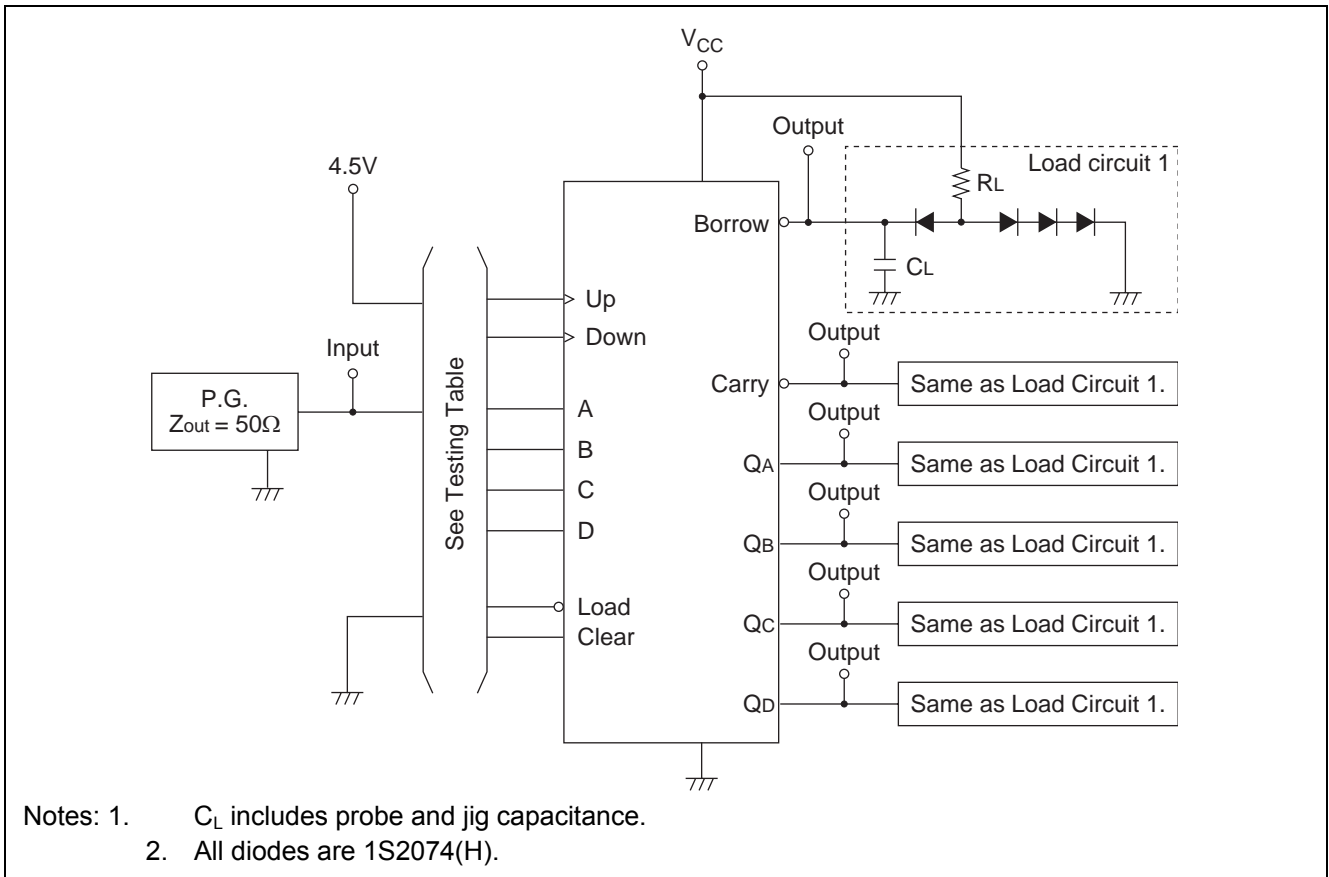
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	$f_{max}$			25	32	—	MHz	
Propagation delay time	$t_{PLH}$ —	Count-up Carry	y		17	26	ns	$C_L = 15 pF, R_L = 2 k\Omega$
	$t_{PHL}$			— 18	24			
	$t_{PLH}$ —	Count-down Borrow	w		16	24	ns	
	$t_{PHL}$			— 15	24			
	$t_{PLH}$ —	Either Count	Q		27	38	ns	
	$t_{PHL}$			— 30	47			
	$t_{PLH}$ —	Load Q			24	40	ns	
	$t_{PHL}$			— 25	40			
$t_{PHL}$ Clear		Q		—	23	35	ns	

### Count Sequences



## Testing Method

### Test Circuit



### Testing Table

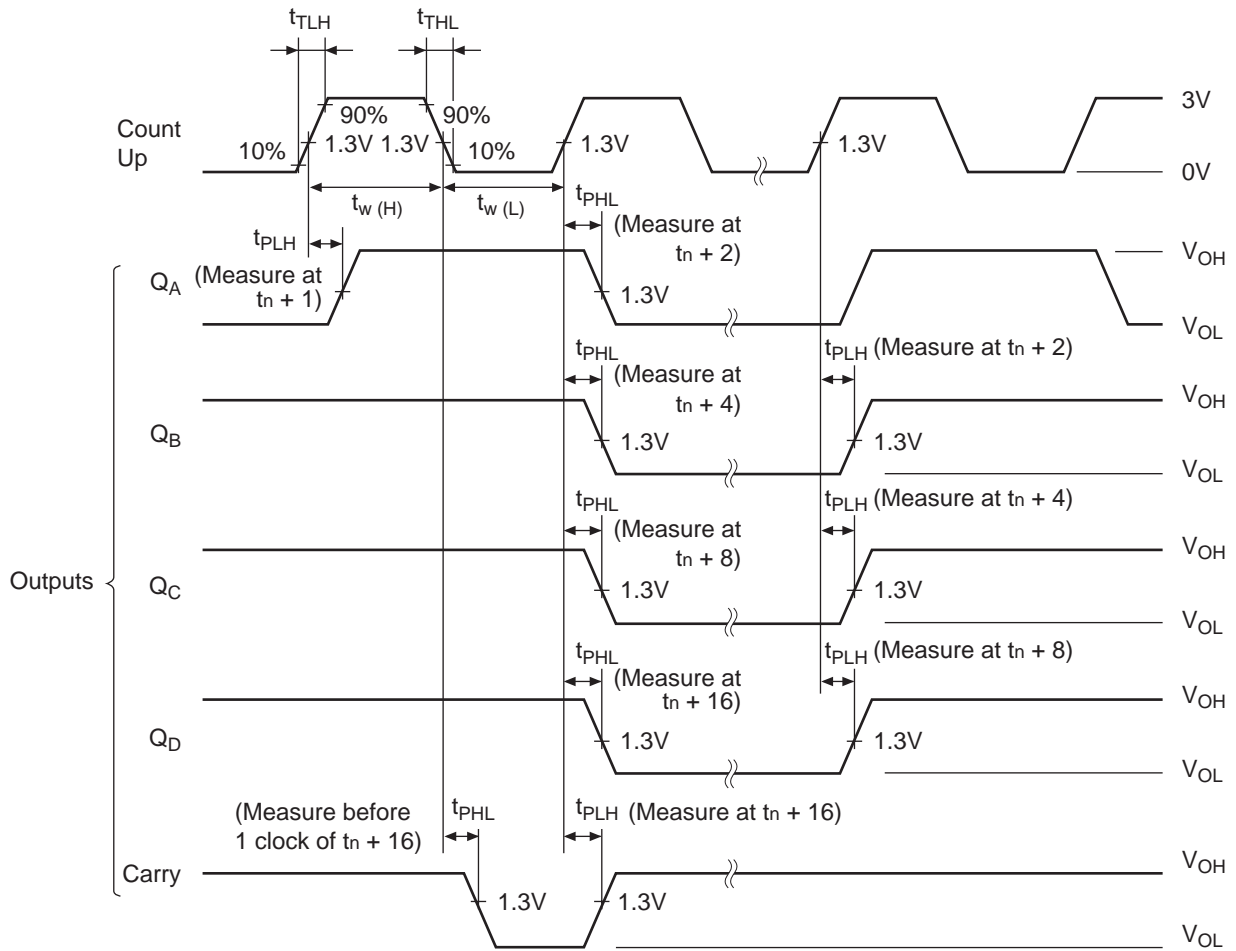
Item	From input to output	Inputs							
		CLR	Load	Up	Down	A	B	C	D
$f_{max}$	Up Count	GND	4.5V	IN	4.5V GND		GND	GND	GND
	Down Count	GND	4.5V	4.5V IN		GND	GND	GND	GND
$t_{PLH}$	Up Count	GND	4.5V	IN	4.5V GND		GND	GND	GND
	Down Count	GND	4.5V	4.5V IN		GND	GND	GND	GND
$t_{PHL}$	Load→Q	GND IN	GND		GND IN		IN	IN	IN
	Clear→Q	IN	IN*	GND	GND	4.5V	4.5V 4.5V	4.5V	

Note: \*. For initialized

Item	From input to output	Outputs					
		Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Carry	Borrow
$f_{max}$	Up Count	OUT	OUT	OUT	OUT	OUT	—
	Down Count	OUT	OUT	OUT	OUT	—	OUT
$t_{PLH}$	Up Count	OUT	OUT	OUT	OUT	OUT	—
	Down Count	OUT	OUT	OUT	OUT	—	OUT
$t_{PHL}$	Load→Q	OUT	OUT	OUT	OUT	—	—
	Clear→Q	OUT	OUT	OUT	OUT	—	—

Waveforms 1

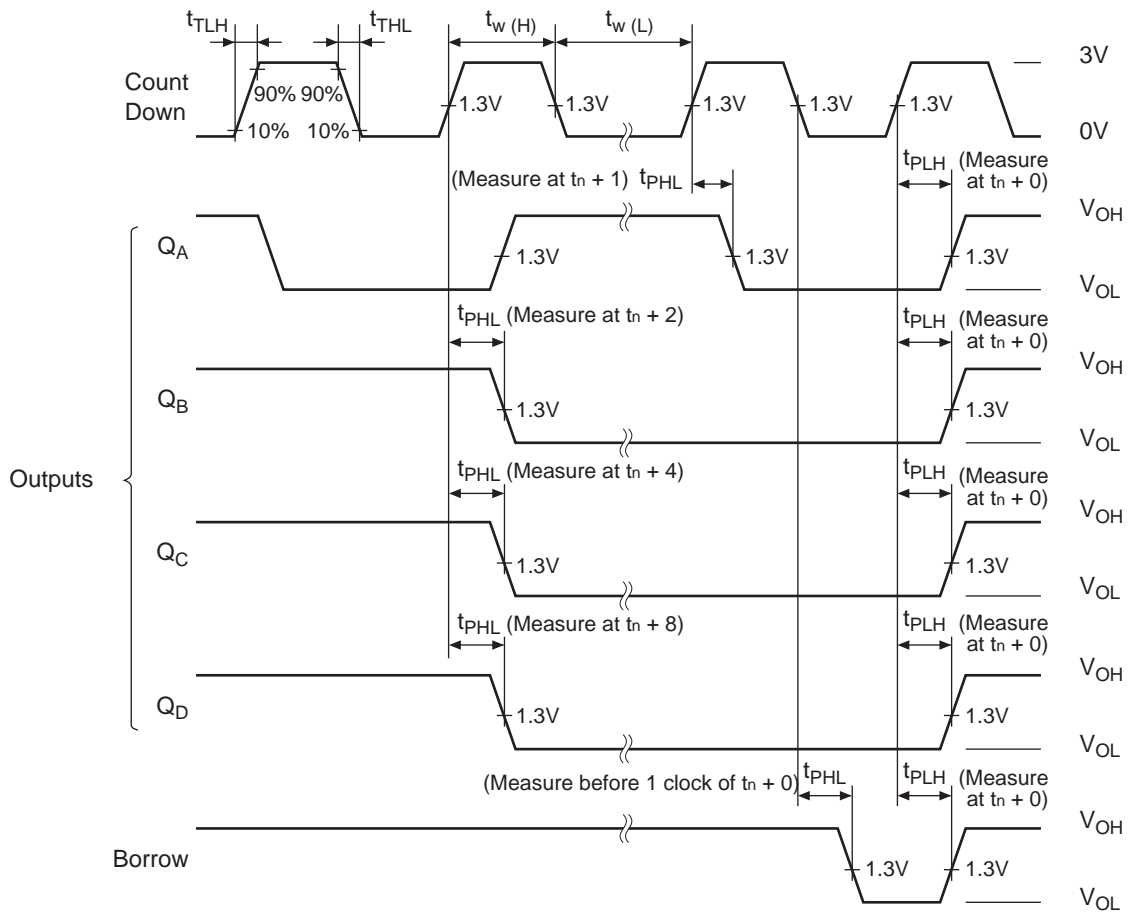
$f_{max}$ ,  $t_{PLH}$ ,  $t_{PHL}$ , (Count Up)



- Notes:
1. Input pulse;  $t_{TLH}$ ,  $t_{THL} \leq 7$  ns, Duty Cycle  $\leq 50\%$ , PRR = 500 kHz (Data input). PRR = 1 MHz (except data input)
  2. for  $f_{max}$   $t_{TLH} = t_{THL} \leq 2.5$  ns.
  3.  $t_n$  is reference bit time when all outputs are low.

Waveforms 2

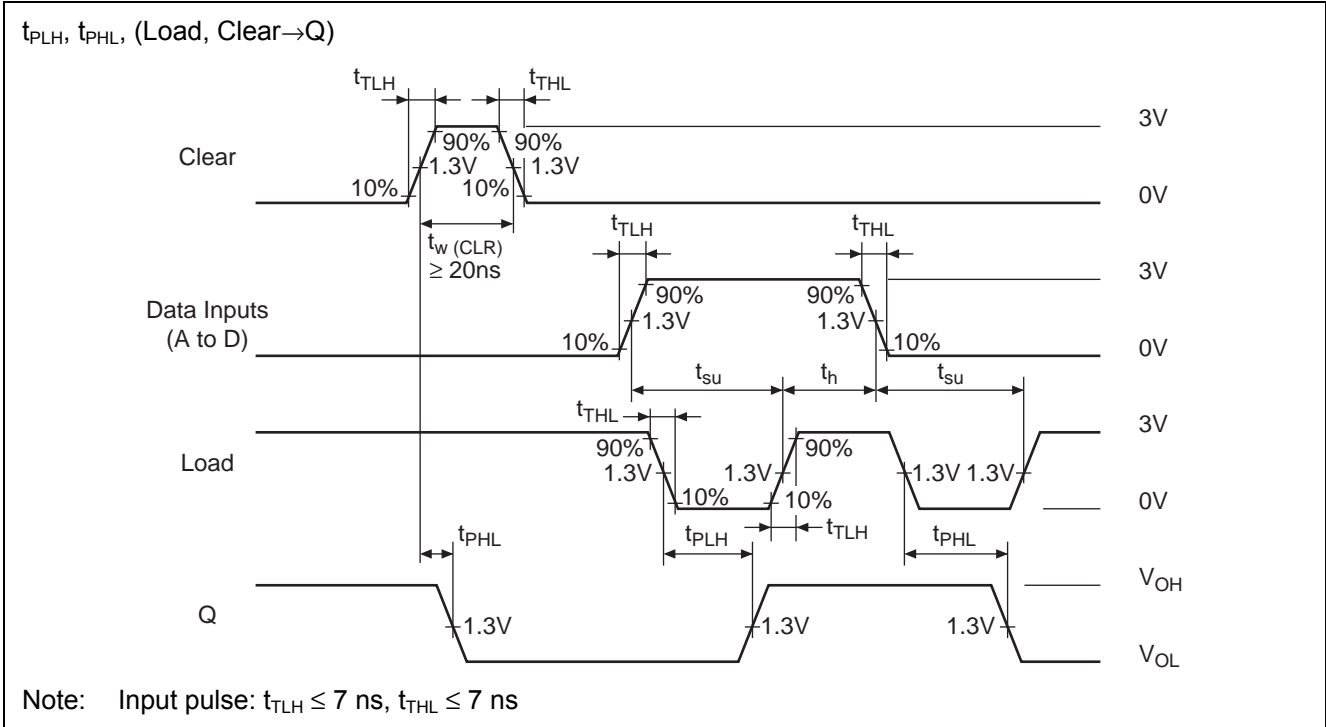
$f_{max}$ ,  $t_{PLH}$ ,  $t_{PHL}$ , (Count Down)



- Notes:
1. Input pulse;  $t_{TLH} \leq 7$  ns,  $t_{THL} \leq 7$  ns, PRR = 1 MHz, duty cycle 50%
  2. for  $f_{max}$   $t_{TLH}$ ,  $t_{THL} \leq 2.5$  ns.
  3.  $t_n$  is reference bit time when all outputs are high.

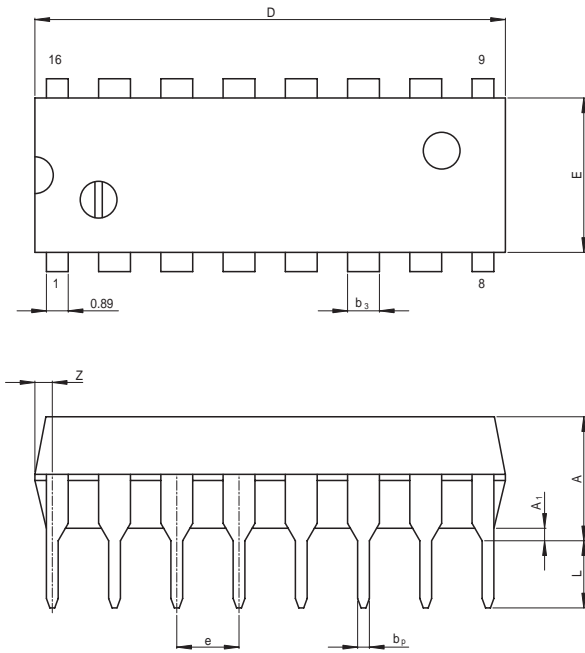


Waveforms 3



Package Dimensions

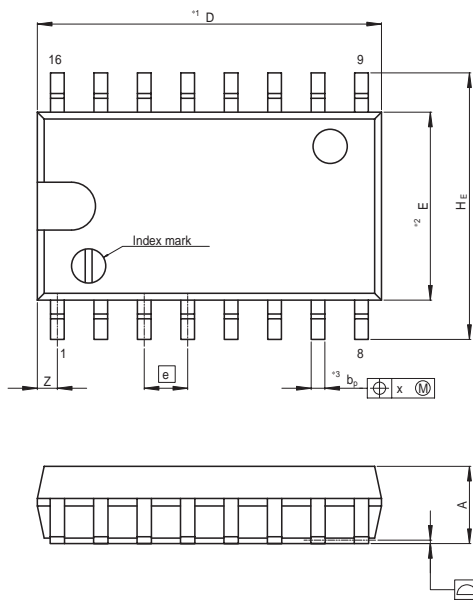
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



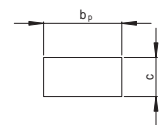
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e <sub>1</sub>	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A <sub>1</sub>	0.51	—	—
b <sub>P</sub>	0.40	0.48	0.56
b <sub>3</sub>	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.12
L	2.54	—	—

( Ni/Pd/Au plating )

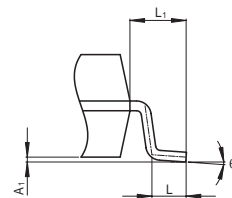
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)  
 1. DIMENSIONS\*1 (Nom)\*AND\*2\*  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION\*3\*DOES NOT  
 INCLUDE TRIM OFFSET.



Terminal cross section  
( Ni/Pd/Au plating )

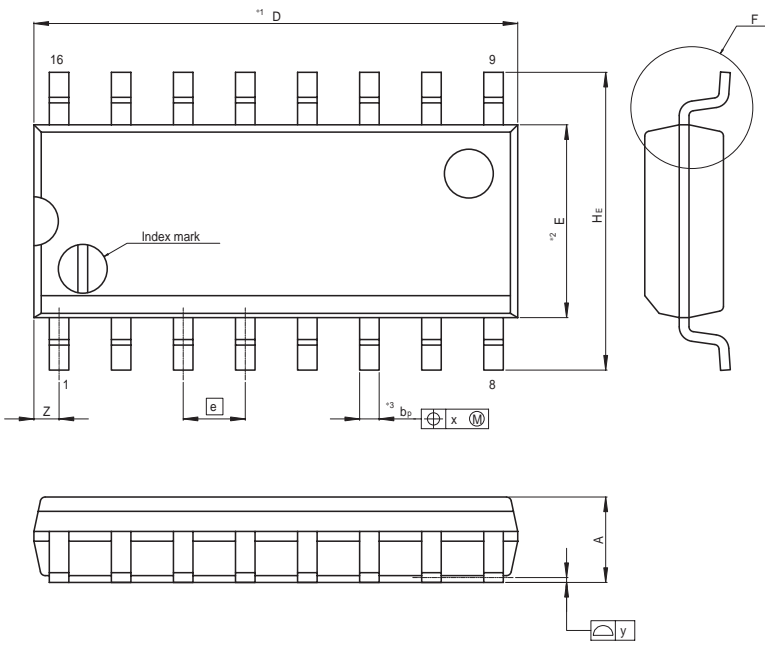


Detail F

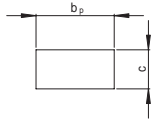
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.00	0.10	0.20
A	—	—	2.20
b <sub>P</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L <sub>1</sub>	—	1.15	—

# HD74LS193

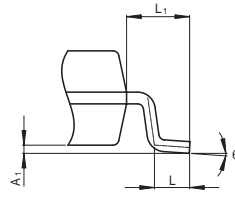
JEITA Package Code P-SOP16-3.95x9.9-1.27	RENESAS Code PRSP0016DG-A	Previous Code FP-16DNV	MASS[Typ.] 0.15g
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NOTE)  
1. DIMENSIONS \*1 (Nom) \*AND\* 2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION \*3\* DOES NOT  
INCLUDE TRIM OFFSET.



Terminal cross section  
( Ni/Pd/Au plating )



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	9.90	10.30
E	—	3.95	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.10	0.14	0.25
A	—	—	1.75
b <sub>p</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
$\theta$	0°	—	8°
H <sub>E</sub>	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.15
Z	—	—	0.635
L	0.40	0.60	1.27
L <sub>1</sub>	—	1.08	—

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