FAIRCHILD SEMICONDUCTOR®

January 2013

LM555
Single Timer

Features

- High-Current Drive Capability: 200 mA
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C
- Timing From µs to Hours
- Turn off Time Less Than 2 µs

Applications

- Precision Timing
- Pulse Generation
- Delay Generation
- Sequential Timing

Description

The LM555 is a highly stable controller capable of producing accurate timing pulses. With a monostable operation, the delay is controlled by one external resistor and one capacitor. With astable operation, the frequency and duty cycle are accurately controlled by two external resistors and one capacitor.

8-DIP

1

8-SOIC

1

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
LM555CN	0 ~ +70°C	LM555CN	DIP 8L	Rail
LM555CM		LM555CM	SOIC 8L	Rail
LM555CMX		LM555CM	SOIC 8L	Tape & Reel

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Block Diagram

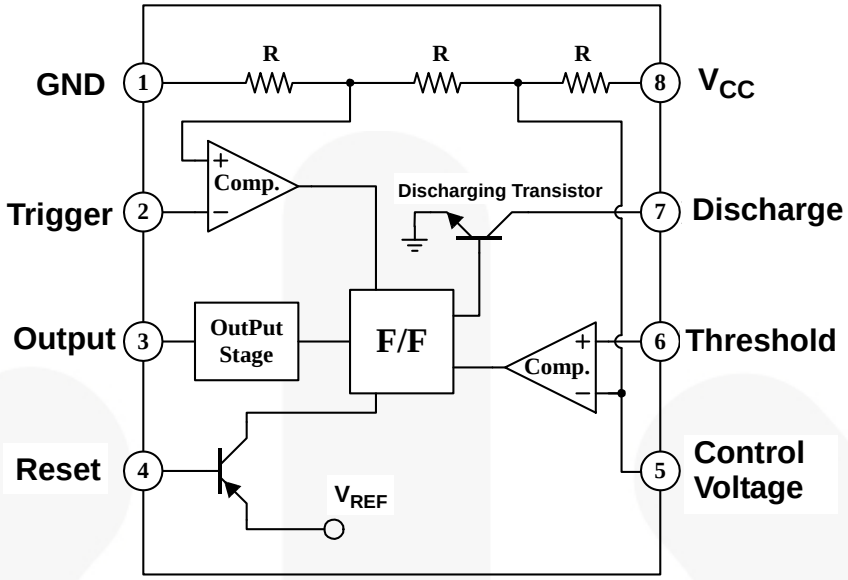

Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	16	V
T_{LEAD}	Lead Temperature (Soldering 10s)	300	°C
P_D	Power Dissipation	600	mW
T_{OPR}	Operating Temperature Range	0 ~ +70	°C
T_{STG}	Storage Temperature Range	-65 ~ +150	°C

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Electrical Characteristics

Values are at T_A = 25°C, V_{CC} = 5 ~ 15 V unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		4.5		16.0	V
Supply Current (Low Stable) (1)	I_{CC}	V_{CC} = 5 V, R_L = ∞		3	6	mA
		V_{CC} = 15 V, R_L = ∞		7.5	15.0	mA
Timing Error (Monostable) Initial Accuracy (2)	ACCUR	R_A = 1 kΩ to100 kΩ C = 0.1 µF		1.0	3.0	%
Drift with Temperature (3)	Δt / ΔT			50		ppm / °C
Drift with Supply Voltage (3)	Δt / ΔV_{CC}			0.1	0.5	% / V
Timing Error (Astable) InItial Accuracy (2)	ACCUR	R_A = 1 kΩ to 100kΩ C = 0.1 µF		2.25		%
Drift with Temperature (3)	Δt / ΔT			150		ppm / °C
Drift with Supply Voltage (3)	Δt / ΔV_{CC}			0.3		% / V
Control Voltage	V_C	V_{CC} = 15 V	9.0	10.0	11.0	V
		V_{CC} = 5 V	2.60	3.33	4.00	V
Threshold Voltage	V_{TH}	V_{CC} = 15 V		10.0		V
		V_{CC} = 5V		3.33		V
Threshold Current (4)	I_{TH}			0.10	0.25	µA
Trigger Voltage	V_{TR}	V_{CC} = 5 V	1.10	1.67	2.20	V
		V_{CC} = 15 V	4.5	5.0	5.6	V
Trigger Current	I_{TR}	V_{TR} = 0 V		0.01	2.00	µA
Reset Voltage	V_{RST}		0.4	0.7	1.0	V
Reset Current	I_{RST}			0.1	0.4	mA
Low Output Voltage	V_{OL}	V_{CC} = 15 V, I_{SINK} = 10 mA		0.06	0.25	V
		V_{CC} = 15 V, I_{SINK} = 50 mA		0.30	0.75	V
		V_{CC} = 5 V, I_{SINK} = 5 mA		0.05	0.35	V
High Output Voltage	V_{OH}	V_{CC} = 15 V, I_{SOURCE} = 200 mA		12.5		V
		V_{CC} = 15 V, I_{SOURCE} = 100 mA	12.75	13.30		V
		V_{CC} = 5 V, I_{SOURCE} = 100 mA	2.75	3.30		V
Rise Time of Output(3)	t_R			100		ns
Fall Time of Output(3)	t_F			100		ns
Discharge Leakage Current	I_{LKG}			20	100	nA

Notes:

1. When the output is high, the supply current is typically 1 mA less than at V_{CC} = 5 V.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. These parameters, although guaranteed, are not 100% tested in production.
4. This determines the maximum value of $R_A + R_B$ for 15 V operation, the maximum total R = 20 MΩ, and for 5 V operation, the maximum total R = 6.7 MΩ.

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Application Information

Table 1 below is the basic operating table of 555 timer.

Table 1. Basic Operating Table

Reset (PIN 4)	V_{TR} (PIN 2)	V_{TH} (PIN 6)	Output (PIN 3)	Discharging Transistor (PIN 7)
Low	X	X	Low	ON
High	< 1/3 V_{CC}	X	High	OFF
High	> 1/3 V_{CC}	> 2/3 V_{CC}	Low	ON
High	> 1/3 V_{CC}	< 2/3 V_{CC}	Previous State	

When the low signal input is applied to the reset terminal, the timer output remains low regardless of the threshold voltage or the trigger voltage. Only when the high signal is applied to the reset terminal, the timer's output changes according to threshold voltage and trigger voltage.

When the threshold voltage exceeds 2/3 of the supply voltage while the timer output is high, the timer's internal discharge transistor turns on, lowering the threshold voltage to below 1/3 of the supply voltage. During this time, the timer output is maintained low. Later, if a low signal is applied to the trigger voltage so that it becomes 1/3 of the supply voltage, the timer's internal discharge transistor turns off, increasing the threshold voltage and driving the timer output again at high.

1. Monostable Operation

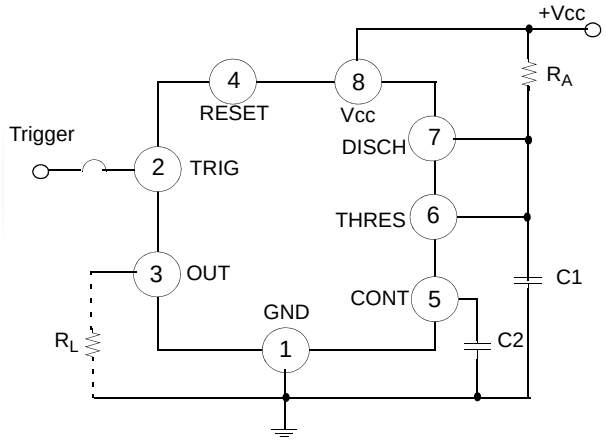

Figure2. Monostable Circuit

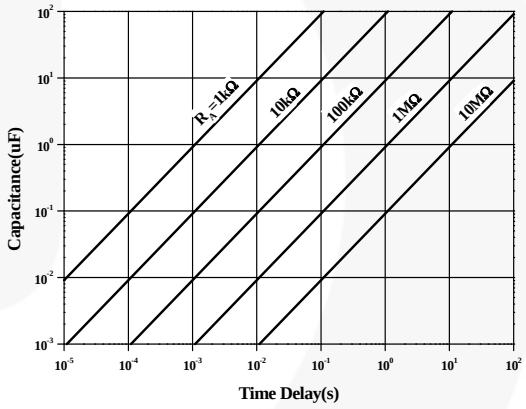

Figure 3. Resistance and Capacitance vs. Time Delay (t_D)

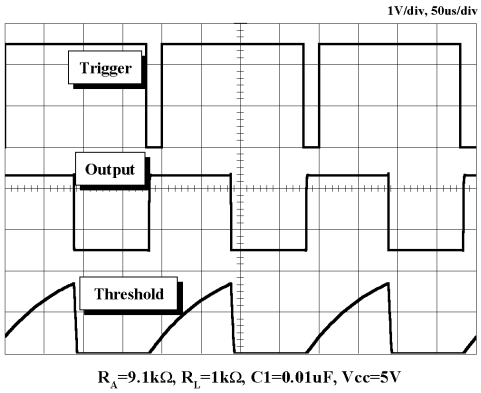

Figure 4. Waveforms of Monostable Operation

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1. Monostable Operation

Figure 2 illustrates a monostable circuit. In this mode, the timer generates a fixed pulse whenever the trigger voltage falls below $V_{CC}/3$. When the trigger pulse voltage applied to the #2 pin falls below $V_{CC}/3$ while the timer output is low, the timer's internal flip-flop turns the discharging transistor off and causes the timer output to become high by charging the external capacitor C1 and setting the flip-flop output at the same time.

The voltage across the external capacitor C1, V_{C1} increases exponentially with the time constant $t = R_A*C$ and reaches $2\ V_{CC}/3$ at $t_D = 1.1\ R_A*C$. Hence, capacitor C1 is charged through resistor R_A. The greater the time constant R_AC, the longer it takes for the V_{C1} to reach $2\ V_{CC}/3$. In other words, the time constant R_AC controls the output pulse width.

When the applied voltage to the capacitor C1 reaches $2\ V_{CC}/3$, the comparator on the trigger terminal resets the flip-flop, turning the discharging transistor on. At this time, C1 begins to discharge and the timer output converts to low. In this way, the timer operating in the monostable repeats the above process. Figure 3 shows the time constant relationship based on R_A and C. Figure 4 shows the general waveforms during the monostable operation.

It must be noted that, for a normal operation, the trigger pulse voltage needs to maintain a minimum of $V_{CC}/3$ before the timer output turns low. That is, although the output remains unaffected even if a different trigger pulse is applied while the output is high, it may be affected and the waveform does not operate properly if the trigger pulse voltage at the end of the output pulse remains at below $V_{CC}/3$. Figure 5 shows such a timer output abnormality.

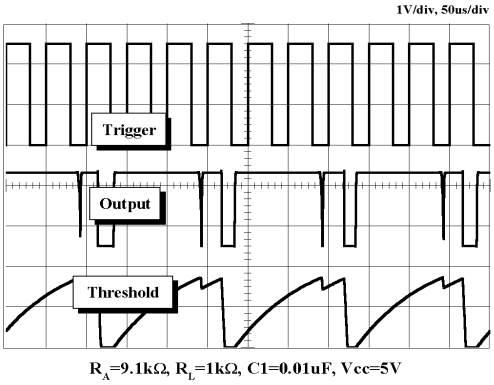

Figure 5. Waveforms of Monostable Operation (abnormal)

2. Astable Operation

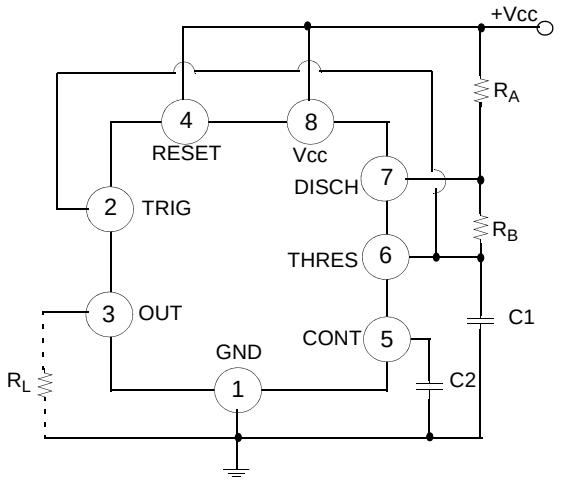

Figure 6. A Stable Circuit

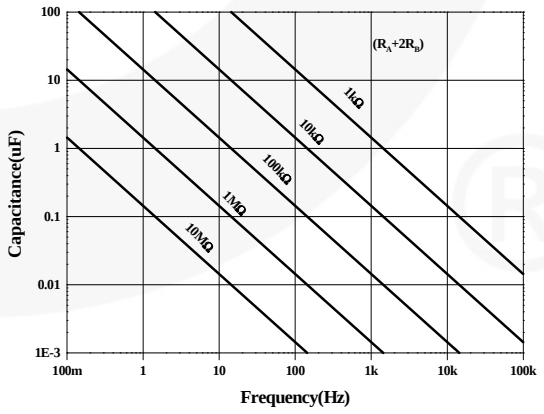

Figure 7. Capacitance and Resistance vs. Frequency

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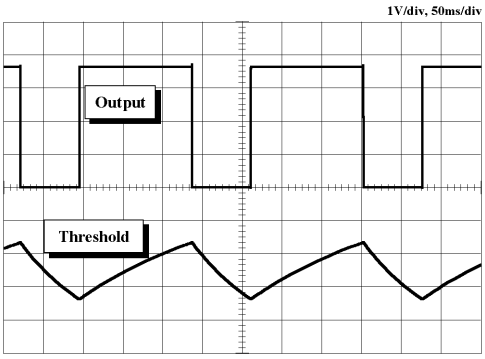
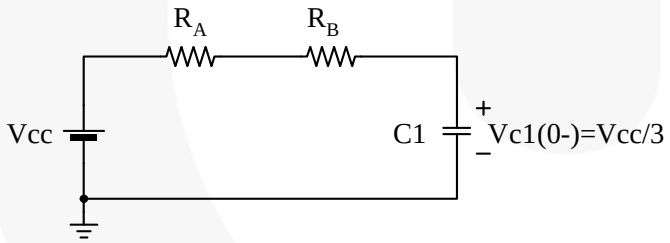


Figure 8. Waveforms of Astable Operation

An astable timer operation is achieved by adding resistor R_B to Figure 2 and configuring as shown on Figure 6. In the astable operation, the trigger terminal and the threshold terminal are connected so that a self-trigger is formed, operating as a multi-vibrator. When the timer output is high, its internal discharging transistor. turns off and the V_{C1} increases by exponential function with the time constant $(R_A+R_B)*C$.

When the V_{C1}, or the threshold voltage, reaches 2 V_{CC}/3; the comparator output on the trigger terminal becomes high, resetting the F/F and causing the timer output to become low. This turns on the discharging transistor and the C1 discharges through the discharging channel formed by R_B and the discharging transistor. When the V_{C1} falls below V_{CC}/3, the comparator output on the trigger terminal becomes high and the timer output becomes high again. The discharging transistor turns off and the V_{C1} rises again.

In the above process, the section where the timer output is high is the time it takes for the V_{C1} to rise from V_{CC}/3 to 2 V_{CC}/3, and the section where the timer output is low is the time it takes for the VC1 to drop from 2 V_{CC}/3 to V_{CC}/3. When timer output is high, the equivalent circuit for charging capacitor C1 is as follows:



$$C_1\frac{dv_{c1}}{dt} = \frac{V_{cc} - V(0\text{-})}{R_A + R_B} \qquad (1)$$

$$V_{C1}(0+) = V_{CC}/3 \qquad (2)$$

$$V_{C1}(t) = V_{CC}\left(1 - \frac{2}{3}e^{-\left(-\frac{t}{(R_A+R_B)C1}\right)}\right) \qquad (3)$$

Since the duration of the timer output high state (t_L) is the amount of time it takes for the $V_{C1}(t)$ to reach 2 V_{CC}/3,

$$V_{C1}(t) = \frac{2}{3}V_{CC} = V_{CC}\left(1 - \frac{2}{3}e^{-\left(-\frac{t_H}{(R_A+R_B)C1}\right)}\right) \qquad (4)$$

$$t_H = C_1(R_A + R_B)\ln 2 = 0.693(R_A + R_B)C_1 \qquad (5)$$

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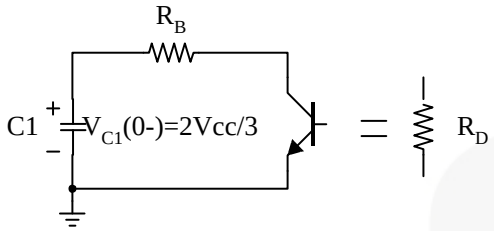
The equivalent circuit for discharging capacitor C1, when timer output is low is, as follows:



$$C_1 \frac{dv_{C1}}{dt} + \frac{1}{R_A + R_B} V_{C1} = 0 \qquad (6)$$

$$V_{C1}(t) = \frac{2}{3} V_{CC} e^{-\frac{t}{(R_A + R_D)C1}} \qquad (7)$$

Since the duration of the timer output low state (t_L) is the amount of time it takes for the VC1(t) to reach $V_{CC}/3$,

$$\frac{1}{3} V_{CC} = \frac{2}{3} V_{CC} e^{-\frac{t_L}{(R_A + R_D)C1}} \qquad (8)$$

$$t_L = C_1(R_B + R_D)\ln 2 = 0.693(R_B + R_D)C_1 \qquad (9)$$

Since R_D is normally $R_B >> R_D$ although related to the size of discharging transistor,

$$t_L = 0.693 R_B C_1 \qquad (10)$$

Consquently, if the timer operates in astable, the period is the same with
'$t = t_H + t_L = 0.693(RA+R_B)C_1 + 0.693R_BC_1 = 0.693(R_A+2R_B)C_1$'
because the period is the sum of the charge time and discharge time. Since frequency is the reciprocal of the period, the following applies:

$$\text{frequency,} \qquad f = \frac{1}{t} = \frac{1.44}{(R_A + 2R_B)C_1} \qquad (11)$$

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3. Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 1 can be made to operate as a frequency divider. Figure 9. illustrates a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

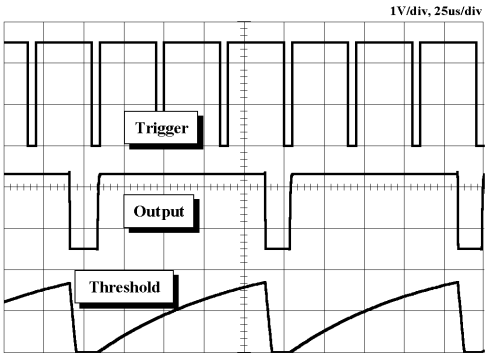

Figure 9. Waveforms of Frequency Divider Operation

4. Pulse Width Modulation

The timer output waveform may be changed by modulating the control voltage applied to the timer's pin 5 and changing the reference of the timer's internal comparators. Figure 10 illustrates the pulse width modulation circuit.
When the continuous trigger pulse train is applied in the monostable mode, the timer output width is modulated according to the signal applied to the control terminal. Sine wave, as well as other waveforms, may be applied as a signal to the control terminal. Figure 11 shows the example of pulse width modulation waveform.

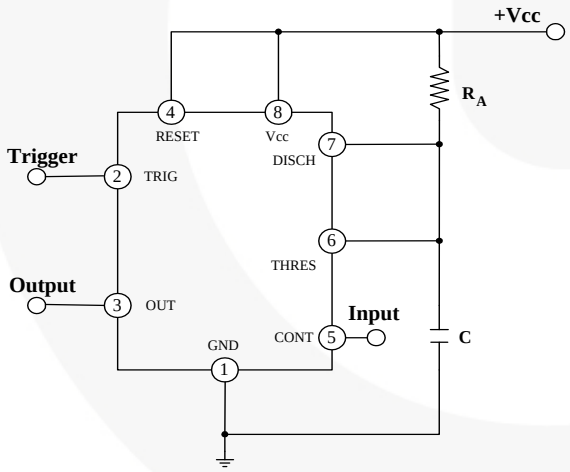

Figure 10. Circuit for Pulse Width Modulation

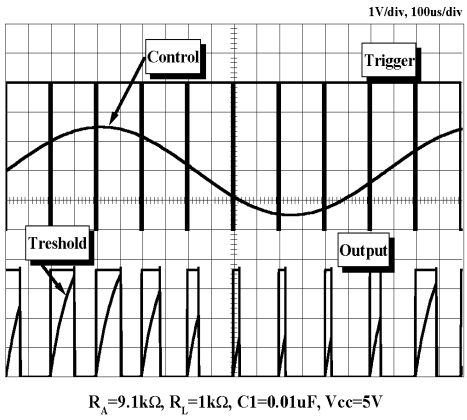

Figure 11. Waveforms of Pulse Width Modulation

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5. Pulse Position Modulation

If the modulating signal is applied to the control terminal while the timer is connected for the astable operation, as in Figure 12, the timer becomes a pulse position modulator.
In the pulse position modulator, the reference of the timer's internal comparators is modulated, which modulates the timer output according to the modulation signal applied to the control terminal.
Figure 13 illustrates a sine wave for modulation signal and the resulting output pulse position modulation; however, any wave shape be used.

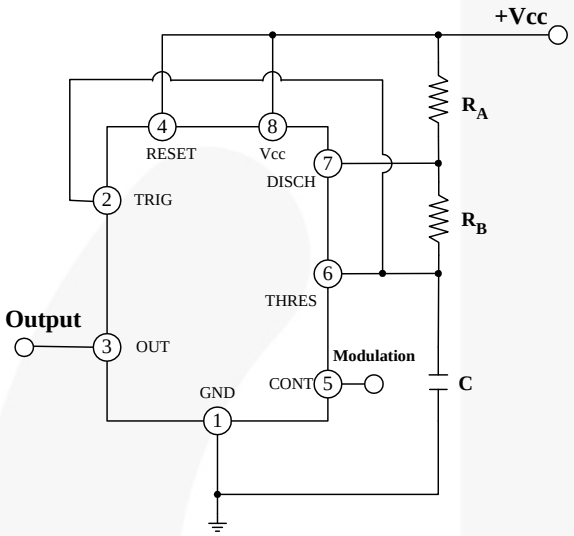

Figure 12. Circuit for Pulse Position Modluation

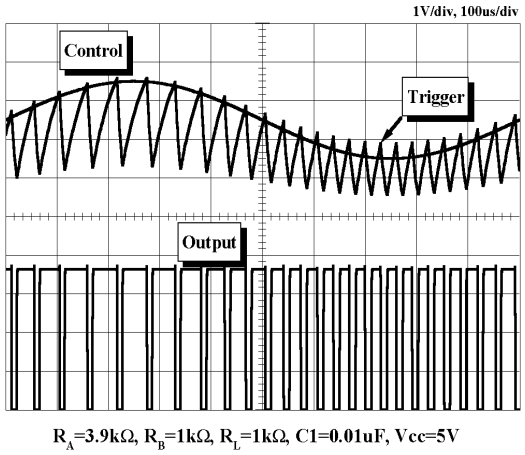

Figure 13. Wafeforms of pulse position modulation

6. Linear Ramp

When the pull-up resistor RA in the monostable circuit shown in Figure 2 is replaced with constant current source, the V_{C1} increases linearly, generating a linear ramp. Figure 14 shows the linear ramp generating circuit and Figure 15 illustrates the generated linear ramp waveforms.

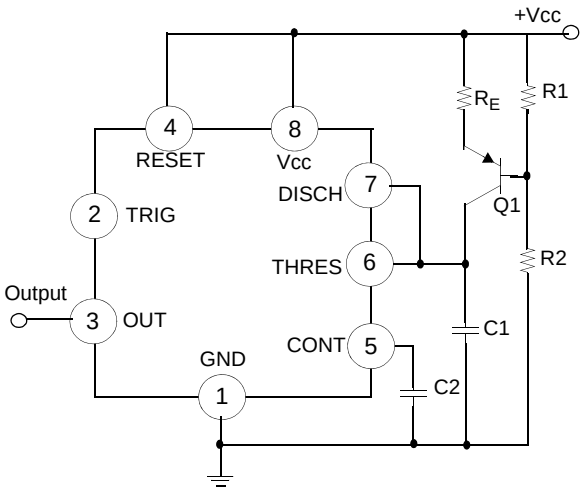

Figure 14. Circuit for Linear Ramp

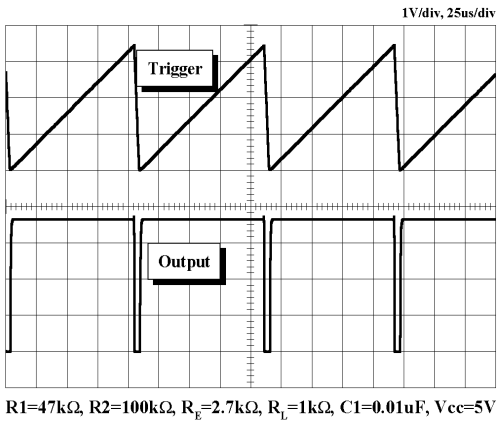

Figure 15. Waveforms of Linear Ramp

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In Figure 14, current source is created by PNP transistor Q1 and resistor R1, R2, and R_E.

$$I_C = \frac{V_{CC} - V_E}{R_E} \qquad (12)$$

Here, V_E is

$$V_E = V_{BE} + \frac{R_2}{R_1 + R_2} V_{CC} \qquad (13)$$

For example, if V_{CC} = 15 V, R_E = 20 kΩ, R1 = 5 kΩ, R2 = 10 kΩ, and V_{BE} = 0.7 V,
V_E=0.7 V+10 V=10.7 V, and
I_C=(15-10.7) / 20 k=0.215 mA.

When the trigger starts in a timer configured as shown in Figure 14, the current flowing through capacitor C1 becomes a constant current generated by PNP transistor and resistors.
Hence, the V_C is a linear ramp function as shown in Figure 15. The gradient S of the linear ramp function is defined as follows:

$$S = \frac{V_{p-p}}{t} \qquad (14)$$

Here the Vp-p is the peak-to-peak voltage.
If the electric charge amount accumulated in the capacitor is divided by the capacitance, the V_C comes out as follows:

$$V = Q/C \qquad (15)$$

The above equation divided on both sides by t gives:

$$\frac{V}{t} = \frac{Q \S t}{C} \qquad (16)$$

and may be simplified into the following equation:

$$S = I/C \qquad (17)$$

In other words, the gradient of the linear ramp function appearing across the capacitor can be obtained by using the constant current flowing through the capacitor.
If the constant current flow through the capacitor is 0.215 mA and the capacitance is 0.02 μF, the gradient of the ramp function at both ends of the capacitor is S = 0.215 m / 0.022 μ = 9.77 V/ms.

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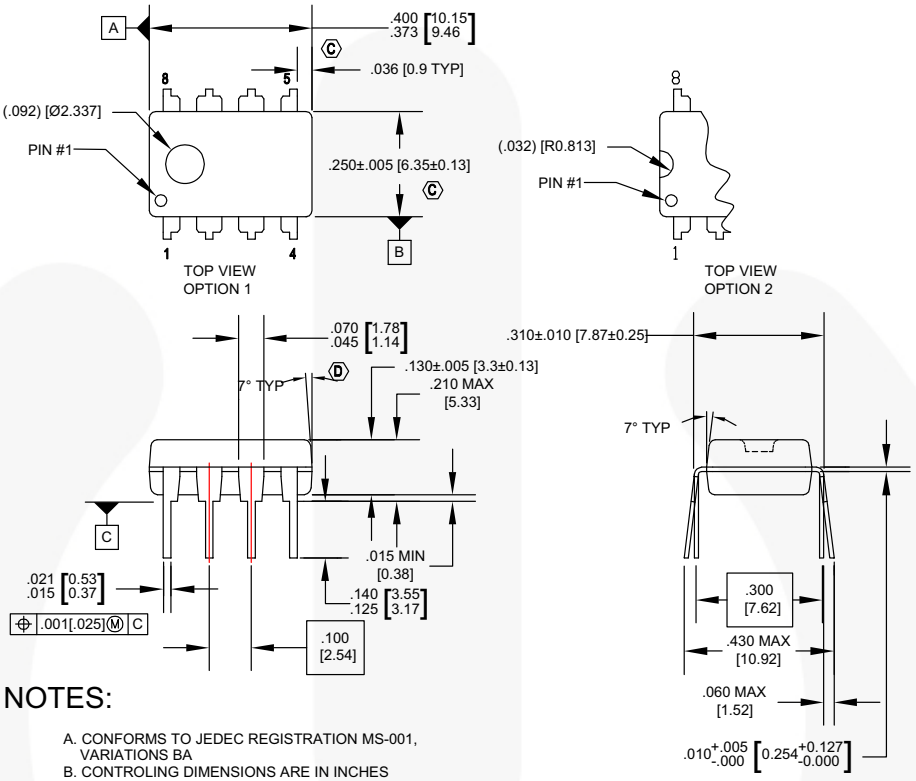
Physical Dimensions

8-DIP



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS BA
B. CONTROLING DIMENSIONS ARE IN INCHES REFERENCE DIMENSIONS ARE IN MILLIMETERS
C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

N08EREVG

Figure 16. 8-Lead, DIP, JEDEC MS-001, 300" WIDE

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Physical Dimensions (continued)

8-SOIC

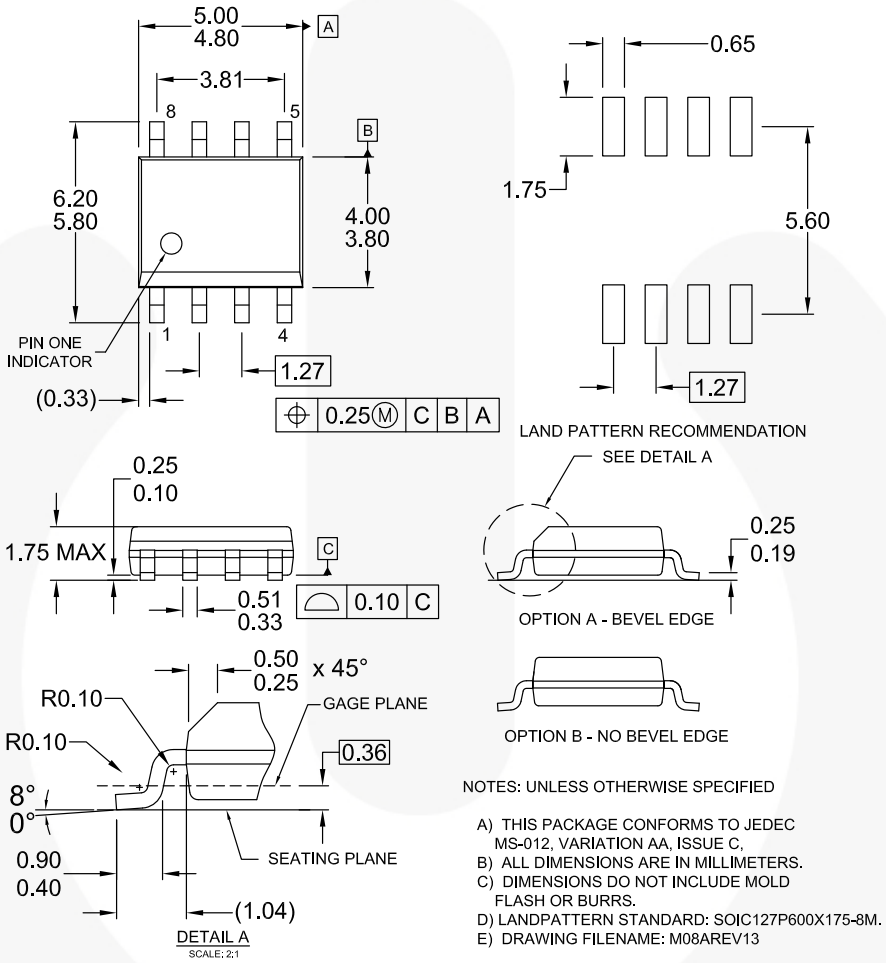

Figure 17. 8-Lead, SOIC,JEDEC MS-012, 150" NARROW BODY

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Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
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SuperSOT™-6
SuperSOT™-8
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