National Semiconductor

August 1992

LMC1983
Digitally-Controlled Stereo Tone and Volume Circuit with Three Selectable Stereo Inputs

General Description

The LMC1983 is a monolithic integrated circuit that provides volume, balance, tone (bass and treble), loudness controls and selection between three pairs of stereo inputs. These functions are digitally controlled through a three-wire communication interface. There are two digital inputs for easy interface to other audio peripherals such as stereo decoders. The LMC1983 is designed for line level input signals (300 mV–2V) and has a maximum gain of −0.5 dB. Volume is set at minimum and tone controls are flat when supply voltage is first applied.

Low noise and distortion result from using analog switches and poly-silicon resistor networks in the signal path.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1983's SELECT OUT/SELECT IN external processor loop.

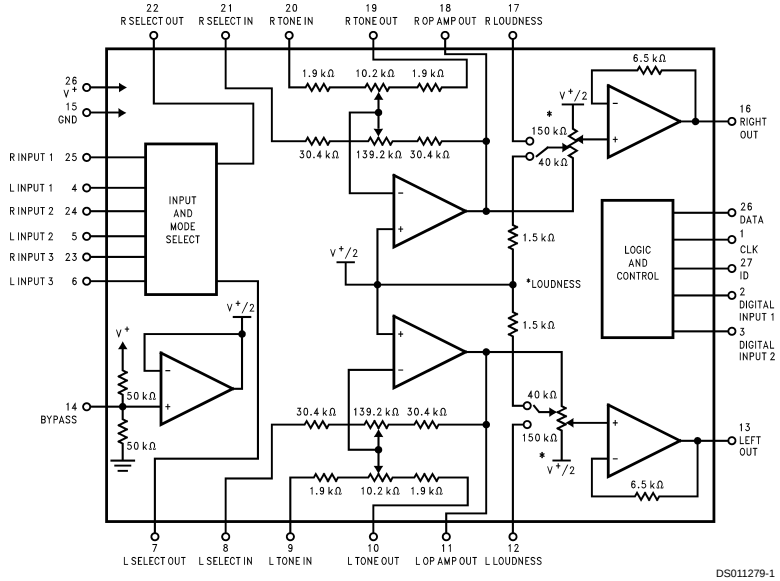
Features

- Low noise and distortion
- Three pairs of stereo inputs
- Loudness compensation
- 40 position 2 dB/step volume attenuator plus mute
- Independent left and right volume controls
- Low noise-suitable for use with DNR® and Dolby® noise reduction
- External processor loop
- Signal handling suitable for compact discs
- Pop-free switching
- Serially programmable: INTERMETAL bus (IM) interface
- 6V to 12V single supply operation
- 28 Pin DIP or PLCC Package

Applications

- Stereo television
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Block Diagram



DS011279-1

DNR® is a registered trademark of National Semiconductor Corporation.
Dolby® is a registered trademark of Dolby Labs.

© 1999 National Semiconductor Corporation

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V^+ − GND)	15V
Voltage at any Pin	GND − 0.2V to V^+ + 0.2V
Input Current at any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Junction Temperature	+125˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature	
N Package, (Soldering, 10 Seconds)	+260˚C
V Package, (Vapor Phase, 60 Seconds)	215˚C
Infrared, (15 Seconds)	220˚C
ESD Susceptability (Note 5)	2 kV

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC1983CIN, LMC1983CIV	−40˚C ≤ T_A ≤ +85˚C
Supply Voltage Range ($V^+ - V^-$)	6V to 12V

Electrical Characteristics

The following specifications apply for V^+ = 9V, f_{IN} = 1 kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J$ = +25˚C.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
I_S	Supply Current		15	25	mA (max)
V_{IN}	Input Voltage	Clipping Level (1.0% THD), Select Out (Pins 7, 22)	2.3	2.0	V_{rms} (min)
THD	Total Harmonic Distortion	Left and Right channels; Output Pins 13, 16			
		V_{IN} = 0.3 V_{rms}; f_{IN} = 100 Hz, 1 kHz, 10 kHz	0.008	0.1	% (max)
		V_{IN} = 2.0 V_{rms}; f_{IN} = 100 Hz, 1 kHz	0.4	1.0	% (max)
		V_{IN} = 2.0 V_{rms}; f_{IN} = 10 kHz	0.5	1.0	% (max)
		V_{IN} = 0.5 V_{rms}; Bass and Treble Tone Controls Set at Maximum	0.07	0.5	% (max)
		V_{IN} = 0.3 V_{rms}; Volume Attenuator at −20 dB, Bass and Treble Tone Controls Set at Maximum	0.06	0.15	% (max)
	DC Shifts	V_{IN} = 0.3 V_{rms}; between Any Two Adjacent Control Settings	2.0	4.0	mV (max)
		V_{IN} = 0.3 V_{rms}; All Mode and Input Positions	18	20	mV (max)
R_{OUT}	AC Output Impedance	Pins 7, 22, (470Ω to Ground at Input)	150	200	Ω (max)
		Pins 13, 16	26	40	Ω (max)
R_{IN}	AC Input Impedance	Pins 4, 5, 23, 24, 25	50	72	kΩ (max)
				35	kΩ (min)
	Volume Attenuator Range	Pins 13, 16; Volume Attenuation at 0100010XXX000000 (0 dB)	0.5	1.5	dB (max)
		0100010XXX101XXX (80 dB); (Relative to Attenuation at the 0 dB Setting)	80	78 82	dB (min) dB (max)
	Volume Step Size	All Volume Attenuation Settings from 0100010XXX101XXX (80 dB) to 0100010XXX000000 (0 dB) (Note 9)	2.0	1.5 2.5	dB (min) dB (min)

Electrical Characteristics (Continued)

The following specifications apply for V^+ = 9V, f_{IN} = 1 kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J$ = +25˚C.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
	Channel-to-Channel Tracking Error	All Volume Attenuation Settings from 0100010XXX100110 (76 dB) to 0100010XXX000000 (0 dB)	±0.1	±1.5	dB (min)
		from 0100010XXX101XXX (80 dB) to 0100010XXX100111 (78 dB)		±2.0	dB (min)
	Mute Attenuation	V_{IN} = 1.0 V_{rms}	105	86	dB (max)
	Bass Gain Range	f_{IN} = 100 Hz, Pins 13, 16	±12	±10.0	dB (min)
				±14.0	dB (max)
	Bass Tracking Error	f_{IN} = 100 Hz, Pins 13, 16	±0.1	±1.5	dB (max)
	Bass Step Size	f_{IN} = 100 Hz, Pins 13, 16	2.0	1.5	dB (min)
		(Relative to Previous Level)		2.5	dB (max)
	Treble Gain Range	f_{IN} = 10 kHz, Pins 13, 16	±12	±10.0	dB (min)
				±14.0	dB (max)
	Treble Tracking Error	f_{IN} = 10 kHz, Pins 13, 16	±0.1	±1.5	dB (max)
	Treble Step Size	f_{IN} = 10 kHz, Pins 13, 16	2.0	1.5	dB (min)
		(Relative to Previous Level)		2.5	dB (max)
	Frequency Response	V_{IN} Applied to Input 1 and Input 2; f_{IN} = 20 Hz − 20 kHz (Relative to Signal Amplitude at 1 kHz)	±0.1	±1.0	dB (max)
	Loudness	Volume Attenuator = 40 dB, Loudness on (See *Figure 5*)			
		Gain at 100 Hz (Referenced to Gain at 1 kHz)	11.5	13.5	dB (max)
				9.5	dB (min)
		Gain at 10 kHz (Referenced to Gain at 1 kHz)	6.5	8.5	dB (max)
				4.5	dB (min)
	Signal-to-Noise Ratio	V_{IN} = 1.0 V_{rms}, A Weighted, Measured at 1 kHz, R_S = 470Ω	95	90	dB (min)
	Channel Balance	All Volume Settings	0.2	1.0	dB (max)
	Channel Separation	Input Pins 4, 25: Output Pins 13, 16; V_{IN} = 1.0 V_{rms} (Note 8)	80	60	dB (min)
	Input-Input Isolation	470Ω to AC Ground on Unused Input	95	60	dB (min)
PSSR	Power Supply Rejection Ratio	V^+ = 9 V_{DC}; 200 mV_{rms}, 100 Hz Sinewave Applied to Pin 26	32	28	dB (min)
f_{CLK}	Clock Frequency		5.0	1.0	MHz (max)
$V_{IN(1)}$	Logic “1” Input Voltage	Pins 1, 27, 28 (IM Bus)	1.3	2.0	V (min)
		Pins 2, 3	2.9	5.5	V (min)
$V_{IN(0)}$	Logic “0” Input Voltage	Pins 1, 27, 28 (IM Bus)	0.4	0.8	V (max)
		Pins 2, 3	1.2	3.5	V (max)
$V_{OUT(1)}$	Logic “1” Output Voltage	Pin 28 (IM Bus)		2.0	V (min)
$V_{OUT(0)}$	Logic “0” Output Voltage	Pin 28 (IM Bus)	0.4	0.8	V (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the deivce may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are specified with respect to ground.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMC1983CIN, T_{JMAX} = +125˚C, and the typical junction-to-ambient thermal resistance, when board mounted, is 67˚C/W.

Electrical Characteristics (Continued)

Note 5: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at T_J = +25°C and represent the most likely parametric norm.

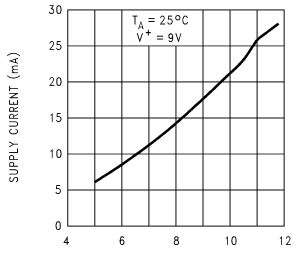
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The Input-Input Isolation is tested by driving one input and measuring the output when the undriven input are selected.

Note 9: The Volume Step Size is defined as the change in attenuation between any two adjacent volume attenuation settings. The nominal Volume Step Size is 2 dB.

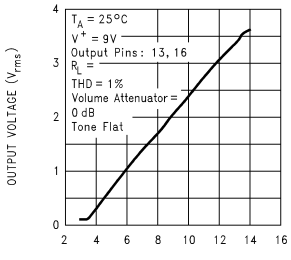
Typical Performance Characteristics

Supply Current vs Supply Voltage



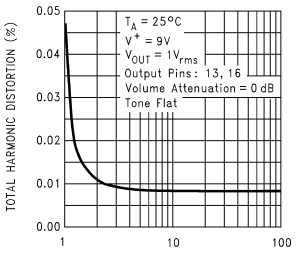
DS011279-11

Output Voltage vs Supply Voltage



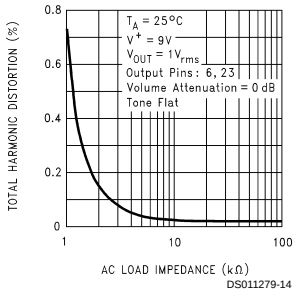
DS011279-12

THD vs Load Impedance



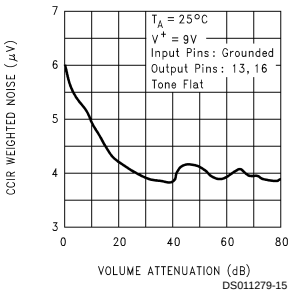
DS011279-13

THD vs Load Impedance



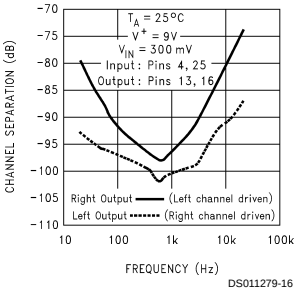
DS011279-14

CCIR Output Noise vs Volume Setting



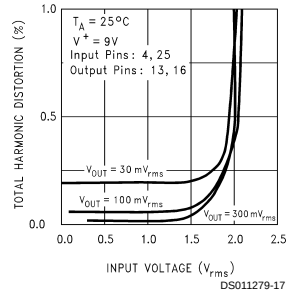
DS011279-15

Channel Separation vs Frequency



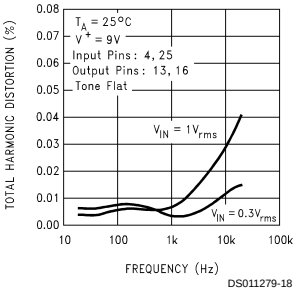
DS011279-16

THD vs V_{IN} (V_{OUT} Constant)



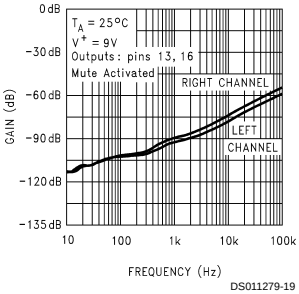
DS011279-17

THD vs Frequency



DS011279-18

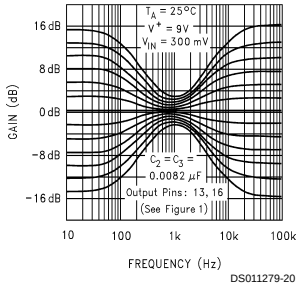
Mute Gain vs Frequency



DS011279-19

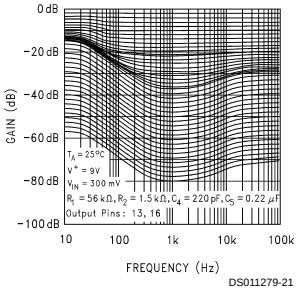
Typical Performance Characteristics (Continued)

Tone Control Response with Equal Bass and Treble Control Settings



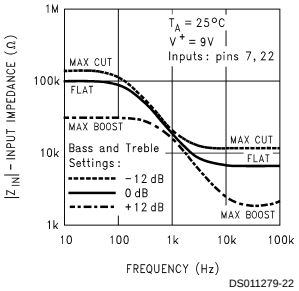
DS011279-20

Loudness Response vs Frequency



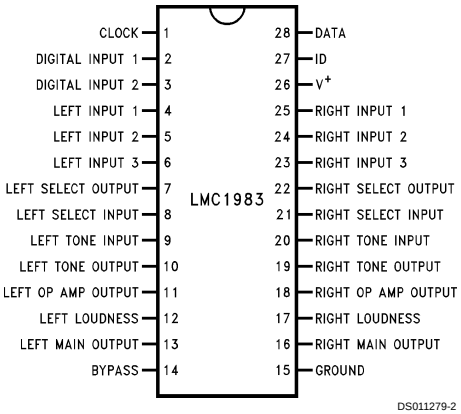
DS011279-21

Select Input Impedance vs Frequency



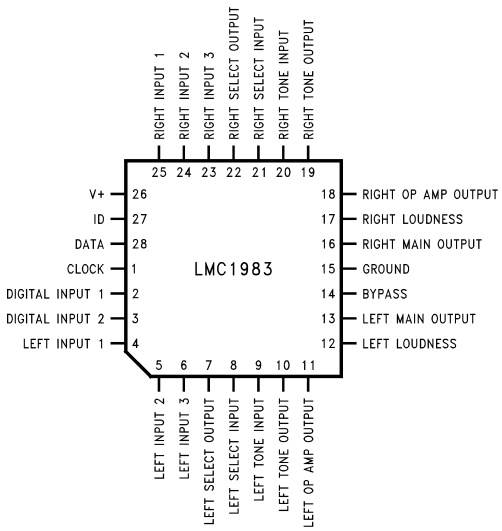
DS011279-22

Connection Diagram



DS011279-2

Top View
Order Number LMC1983CIN
See NS Package Number N28B



DS011279-10

Top View
Order Number LMC1983CIV
See NS Package Number V28A

Pin Description

CLK (1)	The INTERMETAL (IM) Bus clock is applied to the CLOCK pin. This input accepts a TTL or CMOS level signal. The input is used to clock the DATA signal. A data bit must be valid on the rising clock edge.
DIGITAL INPUT 1 & 2 (2, 3)	Internally tied high to V^+ through a 30 kΩ pull-up resistor, these inputs allow a peripheral device to place any single-bit, active low digital information onto the IM Bus. It is then sent out to the controlling device through the DATA pin. Examples of such information could include indication of the presence of a Second Audio Program (SAP) or an FM stereo carrier.
INPUTS 1, 2 & 3 (4, 25; 5, 24; 6, 23)	These are the LMC1983's three stereo input pairs.
SELECT OUT (7, 22)	The selected INPUT signal is available at this output. This feature allows external signal processors such as noise reduction or graphic equalizers to be used. This output can typically sink 1 mA. These pins should be capacitively coupled to pins 8 and 21, respectively, if no external processor is used.
SELECT IN (8, 21)	These are the inputs that an external signal processor uses to return a signal to the LMC1983. These pins should be capacitively coupled to pins 7 and 22, respectively, if no external processor is used.
TONE IN (9, 20)	These are the inputs to the tone control amplifier. See the Application Information section titled "Tone Control Response".
TONE OUT (10, 19)	Tone control amplifier output. See the Application Information section titled "Tone Control Response".
OP AMP OUT (11, 18)	These outputs are used with external tone control capacitors. Internally, this output is applied to the volume attenuators.
LOUDNESS (12, 17)	The output signal on these pins is a voltage taken from the volume attenuator's −40 dB tap point. An external R–C network is connected to these pins.
MAIN OUTPUT (13, 16)	The output signal from these pins drives a stereo power amplifier. The output can typically sink 1 mA.
BYPASS (14)	A 10 µF capacitor is connected between this pin and ground to provide an AC ground for the internal half-supply voltage reference.
GROUND (15)	This pin is connected to analog ground.
V^+ (26)	This is the power supply connection. The LMC1983 is operational with supply voltages from 6V to 12V. This pin should be bypassed to ground through a 1.0 µF capacitor.
ID (27)	This is the IDENTITY digital input that, when low, signals the LMC1983 to receive, from a controlling device, a device address (40_H–47_H), present on the DATA line.
DATA (28)	This is the serial data input for communications sent by a controller. The controller must have open drain outputs used with external pull-up resistors. The data rate has a maximum frequency of 1 MHz. The LMC1983 requires 16 bits of data to control or change a function: the first 8 bits select the LMC1983 and one of eight functions. The final eight bits set the function to a desired value. The data must be valid on the rising edge of the CLOCK input signal.

General Information

The LMC1983 is a CMOS/bipolar building block intended for high fidelity audio signal processing. It is designed for line level inputs signals (300 mV − 2V) and has a maximum gain of −0.5 dB. While the LMC1983 is manufactured with CMOS processing, NPN transistors are used to build low noise op amps. The combination of CMOS switches, bipolar op amps, and poly-silicon resistors make it possible to achieve an order of magnitude quality improvement over other bipolar circuits that use analog multipliers to accomplish gain adjustment. Internal circuits set the volume to minimum, tone controls to flat, the mute to on, and all other functions off when power is first applied. Individual left and right volume controls are software programmed to achieve the stereo balance function. *Figure 1* shows the connection diagram of a typical LMC1983 application.

The LMC1983 has internal decoding logic that allows a microprocessor (µP) or microcontroller (µC) to communicate directly to the audio control circuitry through an INTERMETAL (IM) Bus interface. This three-wire interface consists of a bi-directional DATA line, a Clock (CLK) input line, and an Identity (ID) line. Address and function selection data (8 bits) are serially shifted from the controller to the LMC1983. This is followed by 8 bits of function value data. Data present in the internal shift register is latched and the instruction is executed.

General Information (Continued)

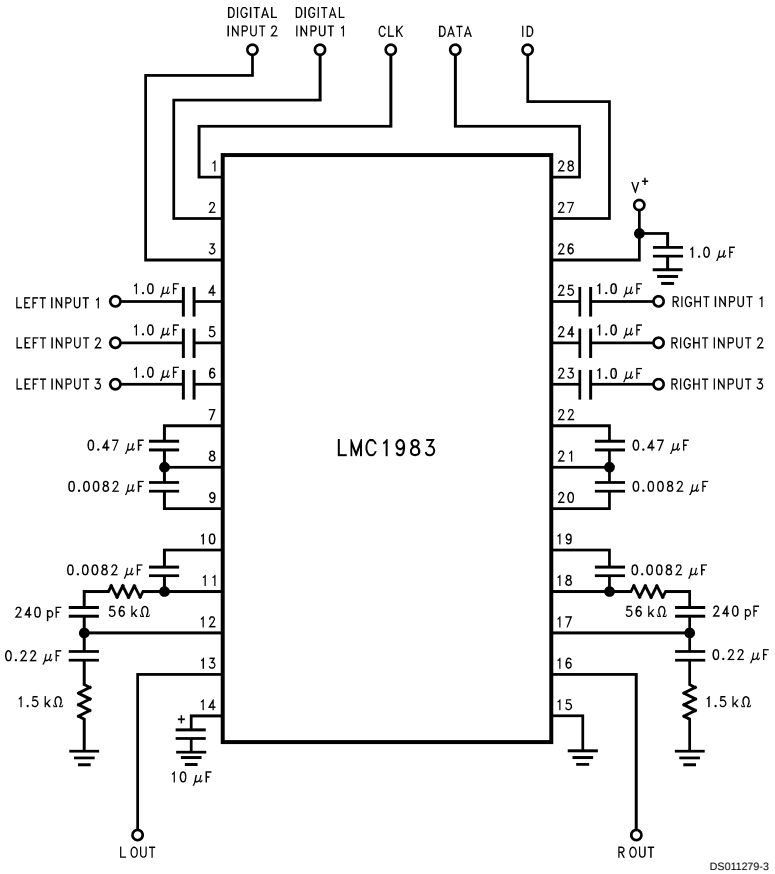


FIGURE 1. Typical Application

Application Information

INPUT SELECTOR

The LMC1983's input selector and mode control are shown in *Figure 2*. The input selector selects one of three stereo signal sources or a mute function with typical attenuation of 100 dB. The selected signals are then sent to a mode control matrix. As shown in *Table 1*, the matrix provides normal stereo or can direct any given channel to both LEFT or RIGHT SELECT OUTPUTs. The third matrix mode is normal stereo. The control matrix output is buffered and appears on each channel's respective SELECT OUT pin (7, 22). Switching noise is kept to a minimum when mute is selected by using a 50 kΩ bias resistor.

Noise performance is optimized through the use of emitter followers in the mode control matrix's output. Internal 50 kΩ resistors are connected to each input selector pin to provide the proper bias point for the emitter follower buffers. Each internal 50 kΩ bias resistor is connected to a common half-supply ($V^+/2$) source. This produces a voltage at pins 7 and 22 (SELECT OUT) that is 1.4V below $V^+/2$ (typically 3.1V with V^+ = 9V). Since a DC voltage is present at the input pins (4, 5, 6, 23, 24, and 25), input signals should be AC coupled through a 1 µF capacitor.

The output signal at pins 7 and 22 can be used to drive exteral audio processing circuits such as noise reduction (LM1894–DNR or Dolby) or graphic equalizers (LMC835). It is important that if any noise reduction is used it be placed ahead of any tone controls or equalizers in the external circuit path to preserve the frequency spectrum of the selected input signal. Otherwise, any frequency equalization could prevent the proper operation of the noise reduction circuit. If no external processor is used, a capacitor should be used to couple the SELECT OUT signals directly to pins 8 and 21, respectively.

MINIMUM LOAD IMPEDANCE

The LMC1983 employs emitter-followers to buffer the selected stereo channels. The buffered signals are available at pins 7 and 22 (SELECT OUT). The SELECT OUT buffers operate with a typical bias current of 1 mA.

The Electrical Specifications table lists a maximum input signal of 2.0 V_{rms} (2.8 V_{peak}) for 1% THD at the SELECT OUT pins. This distortion level is achieved when the minimum AC load impedance seen by the SELECT OUT pins is 2.5 kΩ (2.5V/1 mA). Using lower load impedances results in clipping

Application Information (Continued)

at lower output levels. If the load impedance is DC-coupled, an increased quiescent current can flow. Latch-up may occur if the total emitter current exceeds 5 mA. Thus, maximum output voltage can be increased and much lower distortion levels can be achieved using load impedances of at least 25 kΩ.

INPUT IMPEDANCE

The input impedance of pins 4, 5, 6, 23, 24 and 25 is defined by internal bias resistors and is typically 50 kΩ.

The SELECT IN pins have an input impedance that varies with the BASS and TREBLE control settings. The input impedance is 100 kΩ at DC and 19 kΩ at 1 kHz when the controls are set at 0 dB. Minimum input impedance of 30.4 kΩ at DC and 16 kΩ at 1 kHz occurs when maximum boost is selected. At 10 kHz the minimum input impedance, with the tone controls flat, is 6.8 kΩ and, with the tone controls at maximum boost, is 2.5 kΩ.

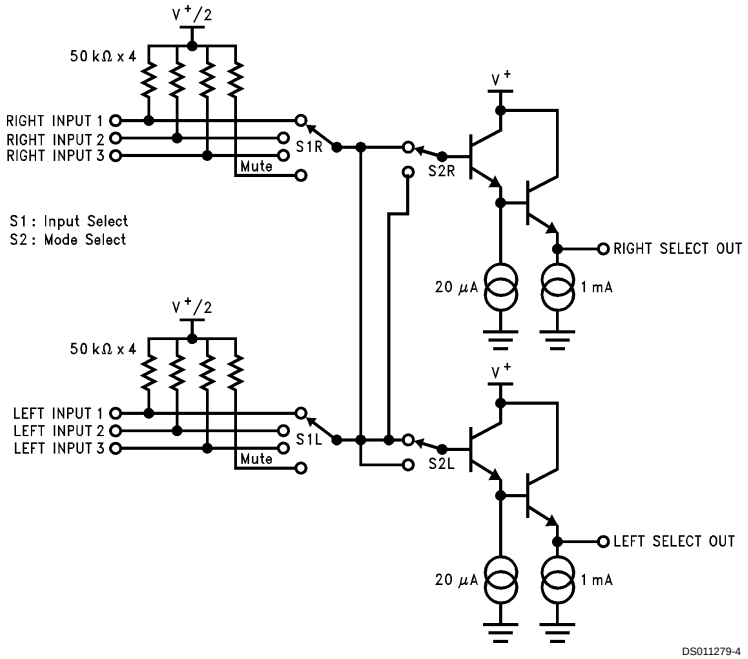


FIGURE 2. Input and Mode Select Circuitry

Application Information (Continued)

TABLE 1. IM Bus Programming Codes for LMC1983

Address (A7–A0)	Function	Data	Function Selected
01000000	Input Select + Mute	XXXXXX00	INPUT1
		XXXXXX01	INPUT2
		XXXXXX10	INPUT3
		XXXXXX11	MUTE
01000001	Loudness	XXXXXXX0	Loudness **OFF**
		XXXXXXX1	Loudness **ON**
01000010	Bass	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000011	Treble	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000100	Left Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000101	Right Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000110	Mode Select	XXXXX100	Left Mono
		XXXXX101	Stereo
		XXXXX11X	Right Mono
01000111	Read Digital Input 1 or Digital Input 2 on IM Bus	XXXXXXD1D0	D0 = Digital Input 1 D1 = Digital Input 2

Application Information (Continued)

EXTERNAL SIGNAL PROCESSING

The SELECT OUT pins (7 and 22) enable greater system design flexibility by providing a means to implement an external processing loop. This loop can be used for noise reduction circuits such as DNR (LM1894) or multi-band graphic equalizers (LMC835). If both are used, it is important to ensure that the noise reduction circuitry precede the equalization circuits. Failure to do so results in improper operation of the noise reduction circuits. The system shown in *Figure 3* utilizes the external loop to include DNR and a multi-band equalizer.

TONE CONTROL RESPONSE

Bass and treble tone controls are included in the LMC1983. The tone controls use just two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 (see *Figure 4*) and internal resistors in the feedback loop of the internal tone amplifier. The maximum-boost or cut is determined by the data sent to the LMC1983 (see *Table 1*).

The typical tone control response shown in Typical Performance Curves were generated with C2 = C3 = 0.0082 µF and show the response for each step. When modifying the tone control response it is important to note that the ratio of C3 and C2 sets the mid-frequency gain. Symmetrical tone response is achieved when C2 = C3. However, with C2 = 2(C3) and the tone controls set to "flat", the frequency response will be flat at 20 Hz and 20 kHz, and +6 dB at 1 kHz.

The frequency where a tone control begins to deviate from a flat response is referred to as the turn-over frequency. With C = C2 = C3, the LMC1983's treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi C(14\ k\Omega)}$$

The bass turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi C(30.4\ k\Omega)}$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are for treble and bass

$$f_{TI} = \frac{1}{2\pi C(1.9\ k\Omega)}$$

$$f_{BI} = \frac{1}{2\pi C(169.6\ k\Omega)}$$

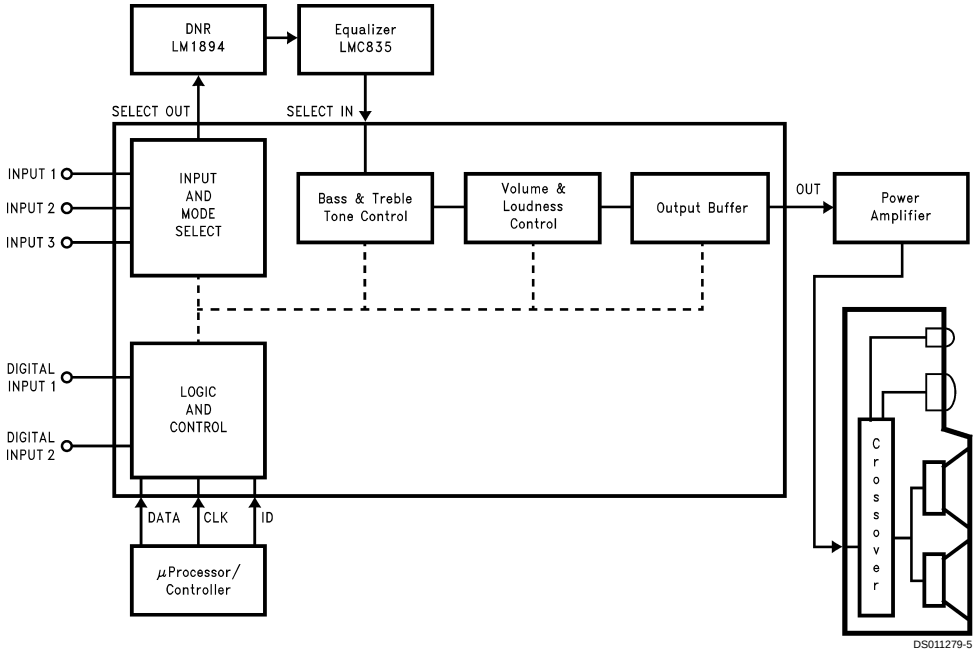


FIGURE 3. System Block Diagram Utilizing the External Processing Loop (One Channel Shown)

Application Information (Continued)

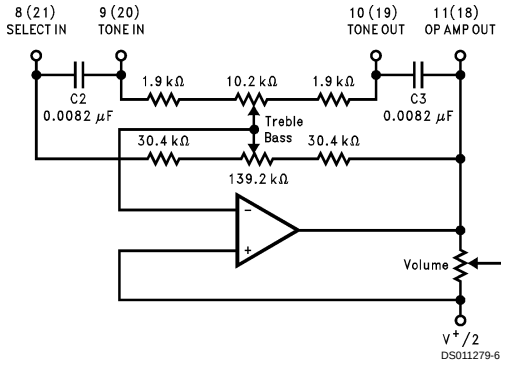


FIGURE 4. The Tone Control Amplifier

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Curves will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 µF shifts the 2 dB per step frequency to 72 Hz and 8.3 kHz. If the tone control capacitors' size is decreased these frequencies will increase. With C2 = C3 = 0.0068 µF the 2 dB steps take place at 130 Hz and 11.2 kHz.

LOUDNESS

The human ear has less sensitivity to high and low frequencies relative to its sensitivity to mid-range frequencies between 2 kHz and 6 kHz for any given acoustic level. The low and high frequency sensitivity decreases faster than the sensitivity to the mid-range frequencies as the acoustic level drops. The LMC1983's loudness function can be used to help compensate for the decreased sensitivity by boosting the gain at low and high frequencies as the volume control attenuation increases (see the curve labeled "Gain vs Frequency with Loudness Active").

The LMC1983's loudness function uses external components R1, R2, C4 and C5, as shown in *Figure 5*, to select the frequencies where bass and treble boost begin. The amount of boost is dependent on the volume attenuator's setting. The loudness characteristic, with the volume attenuator set at 40 dB, has a transfer function of

$$\frac{V_0}{V_I} = \frac{(sC5R2 + 1)[sC4(R1 + 156k) + 1]}{(s^2)C4C5R2(163k) + s[C4(156k) + C5(4.9R2 + 156k)] + 1}$$

The external components R1 and C4 can be eliminated and pin 11(18) left open if bass boost is the only desired loudness characteristic.

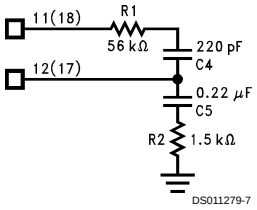


FIGURE 5. Loudness Control Circuit

SERIAL DATA COMMUNICATION

The LMC1983 uses the INTERMETAL serial bus (IM Bus) standard. Serial data information is sent to the LMC1983 over a three wire IM Bus consisting of Clock (CLK), Data (DATA), and Identity (ID). The DATA line is bidirectional and the CLK and ID lines are unidirectional from the microprocessor or micontroller to the LMC1983. The LMC1983's bidirectional capability is accomplished by using an open drain output on the DATA line and an external 1 kΩ pull-up resistor.

The LMC1983 responds to address values from 01000000 (40_H) through 01000111 (47_H). The addresses select one of the eight available functions (see *Table 1*). The IM Bus' lines have a logic high standby state when using TTL logic levels. As shown in *Figure 6*, data transmission is initiated by low levels on CLK and ID. Next, eight address bits are sent. This address information includes the code to select one of the LMC1983's desired functions. Each address bit is clocked in on the rising edge of CLK. The ID line is taken high after the eight bits of address data are received by the LMC1983.

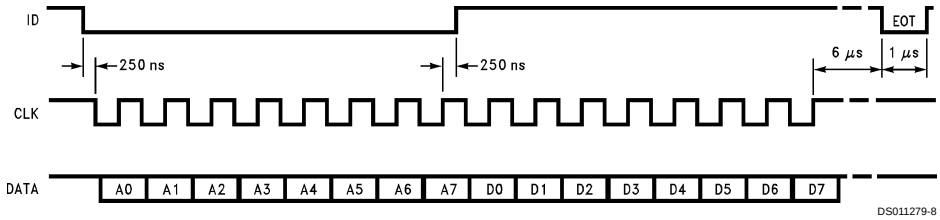


FIGURE 6. LMC1983's INTERMETAL Serial Bus Timing

The controlling system continues toggling the CLK line eight more times. Data that determines the selected function's operating point is written into, or single bit information on DIGITAL INPUT 1 or DIGITAL INPUT 2 is read from, the LMC1983. Finally, the end of transmission is signaled by pulsing the ID line low for a minimum of 3 µs. The transmitted function data is latched and the function changes to its new setting.

Table 1 also details the serial data structure, range, and bit assignments that sets each function's operating point. The volume and tone controls' function control data binarily increments from zero to maximum as the function's operating point changes from 80 dB attenuation to 0 dB attenuation (volume) or −12 dB to +12 dB (tone controls). Note that not all data bits are needed by each function. The extra bits shown as "X"s ("don't cares") are position holders and have

Application Information (Continued)

no affect on a respective control. They are necessary to properly position the data in the LMC1983's internal data shift register. Unexpected results may take place if these bits are not sent.

The LMC1983's internal data shift register can handle either a 16-bit word or two 8-bit serial data transmissions. It is the final 8 bits of data received before the ID line goes high that are used as the LMC1983 selection and function addresses. The final eight bits after the ID line returns high are used to change a function's operating point. CLK must be stopped when the final 8 data bits are received. The data stored in the internal data latch remains unchanged until the ID is pulsed, signifying the end of data transmission. When ID is pulsed, the new data in the data shift register is latched into the data latch and the selected function takes on a new operating point.

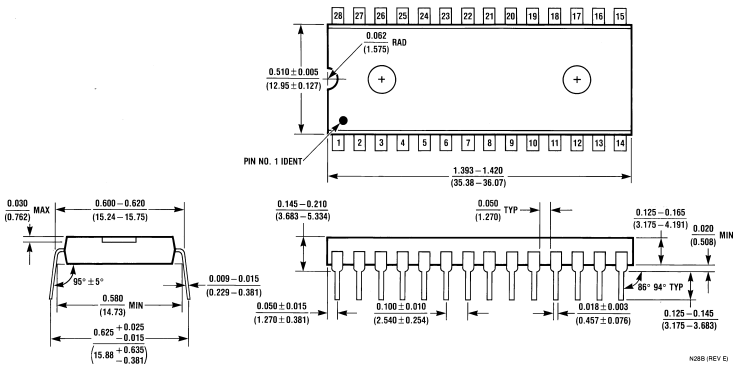
A complete description and more information concerning the IM Bus is given in the appendix of ITT's CCU2000 datasheet.

DIGITAL I/O

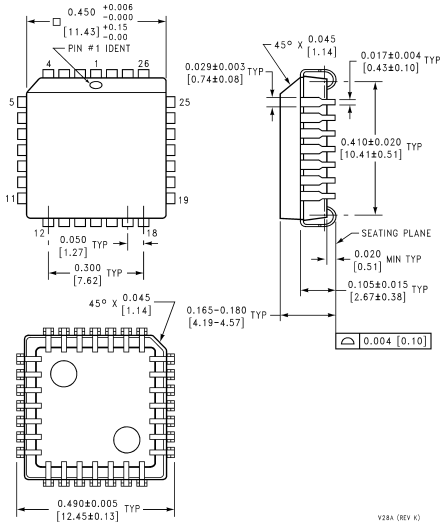
The LMC1983's two Digital Input pins, 2 and 3, provide single-bit communication between a peripheral device and the controller over the IM Bus. Each pin has an internal 30 kΩ pull-up resistor. Therefore, these pins should be connected to open collector/drain outputs. The type of information that could be received on these lines and retrieved by a controller include FM stereo pilot indication, power on/off, Secondary Audio Program (SAP), etc.

According to *Table 1*, the logic state of DIGITAL INPUT 1 and DIGITAL INPUT 2 is latched and can be retrieved over the IM Bus using the read command (47_H). The single-bit information sent on the IM Bus is active low since these lines are internally pulled high.

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number LMC1983CIN
NS Package Number N28B



Order Number LMC1983CIV
NS Package Number V28A

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated