M74LS175P

QUADRUPLE D-TYPE FLIP FLOP WITH RESET

DESCRIPTION

The M74LS175P is a semiconductor integrated circuit containing 4 positive edge-triggered D-type flip-flops with common clock input T and direct reset input $\overline{R_D}$ and discrete data inputs D.

FEATURES

- Positive edge-triggering
- Clock and direct reset inputs common to 4 circuits
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20~+75°C)

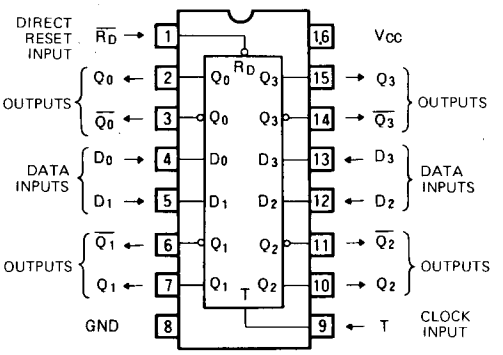
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change emerges in outputs Q and $\overline{Q}$ in accordance with the function table. By setting $\overline{R_D}$ low, all the Q and $\overline{Q}$ outputs are set low and high, respectively, irrespective of the status of the other inputs signals. For use as a D-type flip-flop, $\overline{R_D}$ must be kept in high.

PIN CONFIGURATION (TOP VIEW)



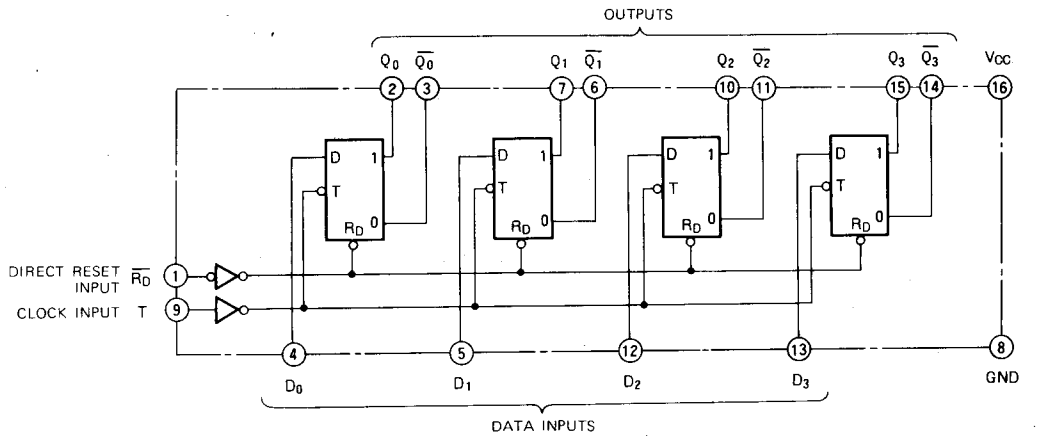
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{R_D}$	T	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

Note 1 X : Irrelevant
↑ : Transition from low to high level (positve edge trigger)
Q_0 : Level of Q before the indicated steady-state input conditions were established.

BLOCK DIAGRAM



QUADRUPLE D-TYPE FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	°C
Tstg	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$ $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$	$I_{OL} = 4mA$		0.25	0.4	V
		$V_I = 0.8V, V_I = 2V$	$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				-0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC} = 5.25V$, $V_O = 0V$		-20		-100	mA
I_{CC}	Supply current	$V_{CC} = 5.25V$ (Note 3)			11	18	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$

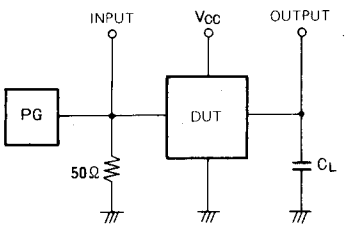
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with 4.5V applied to D and $\overline{R_D}$ after T is set to 0V.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L = 15pF$ (Note 4)	30	50		ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from T to Q, $\overline{Q}$			10	25	ns
t_{PHL}				12	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{R_D}$ to Q, $\overline{Q}$			15	30	ns
t_{PHL}				19	30	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, $t_r \doteq 6ns$, $t_f = 6ns$, $t_w = 500ns$,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance.

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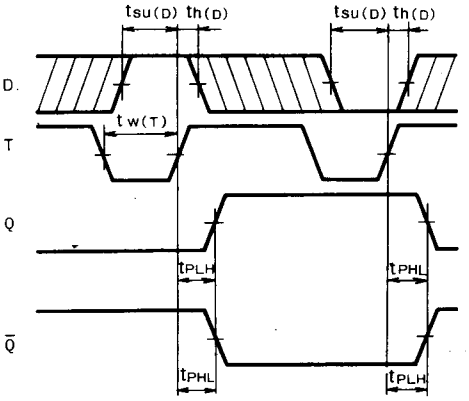
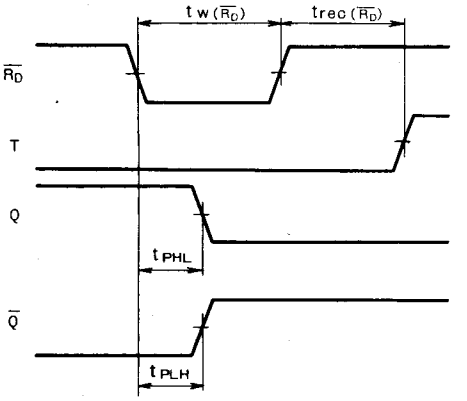
QUADRUPLE D-TYPE FLIP FLOP WITH RESET

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(T)}$	Clock input T pulse width		20	4		ns
$t_{W(\overline{R_D})}$	Direct reset input pulse width		20	7		ns
$t_{SU(D)}$	Setup time high to T		20	2		ns
$t_{h(D)}$	Hold time high to T		5	0		ns
$t_{rec(\overline{R_D})}$	Recovery time for direct reset input		25	5		ns

TIMING DIAGRAM (Reference level = 1.3V)

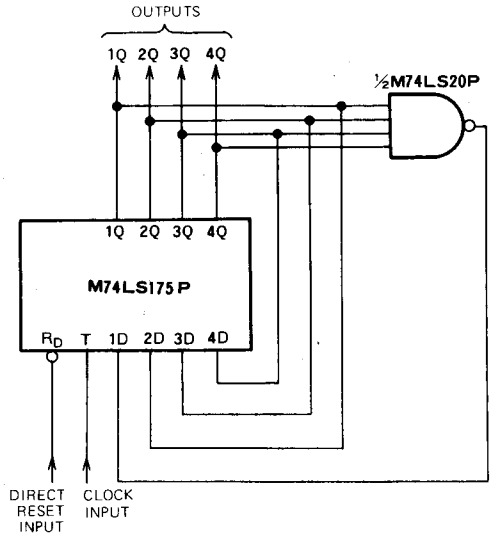


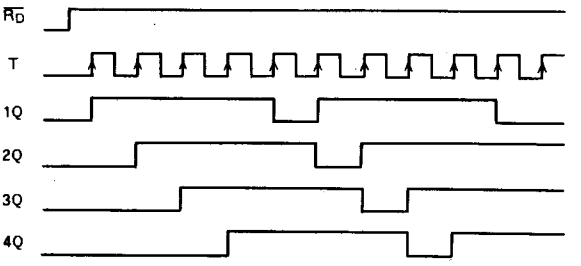


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Timing pulse generator





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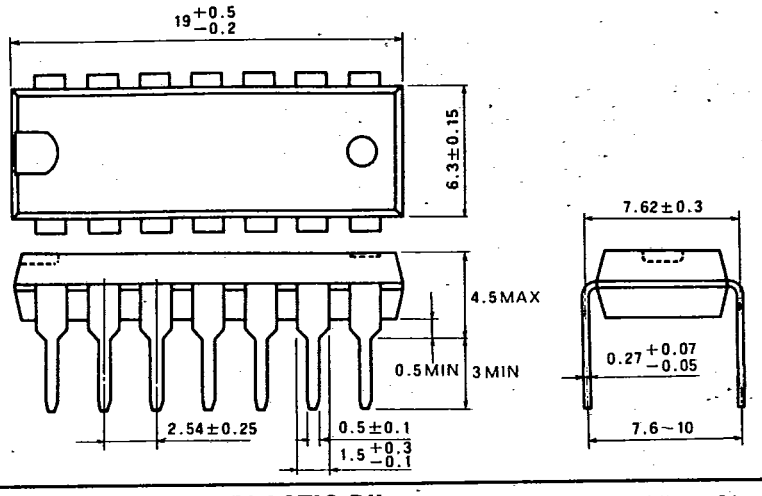
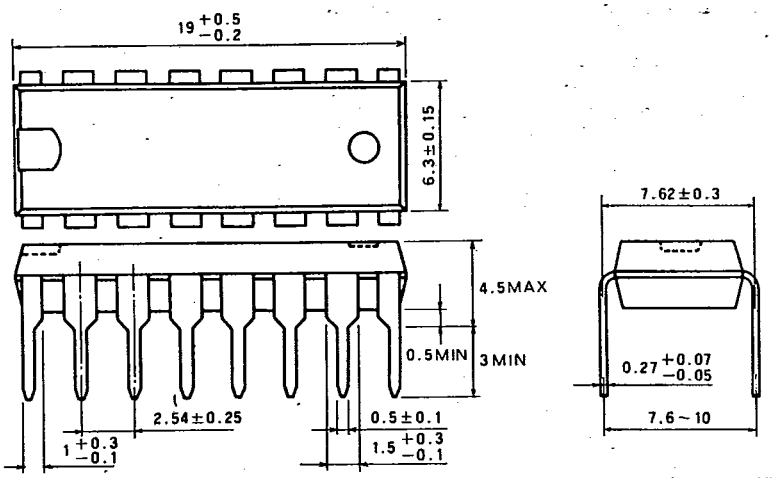
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm