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NTE74HC154
Integrated Circuit
TTL – High Speed CMOS,
4–Line–to–16–Line Decoder/Demultiplexer
24–Lead DIP Type Package

Description:

The NTE74HC154 is a 4–line–to–16–line decoder/demultiplexer in a 24–Lead plastic DIP type package with two enable inputs, E1 and E2. A HIGH on either enable input forces the output into the HIGH state. The demultiplexing function is performed by using the four input lines, A0 to A3, to select the output lines $\overline{Y0}$ to $\overline{Y15}$, and using the one enable as the data input while holding the other enable LOW.

Features:

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{SS} at V_{CC} = 5V
- Two Enable Inputs to Facilitate Demultiplexing and Cascading Functions
- Fanout (Over Temperature Range)
  - Standard Outputs: 10 LS–TTL Loads
  - Bus Driver Outputs: 15 LS–TTL Loads
- Wide Operating Temperature Range: –55° to +125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Maximum Junction Temperature, T_J . . . . . +150°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Typical Thermal Resistance, Junction–to–Ambient (Note 3), R_{thJA} . . . . . 75°C/W
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1. Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. R_{thJA} is measured with the component mounted on an evaluation PC board in free air.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–55	–	+125	°C
Input Rise or Fall Times V_{CC} = 2.0V	t_r, t_f	–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics: (V_{CC} = 5V ±10%, Note 4 unless otherwise specified)

Parameter	Sym-bol	Test Conditions	V_{CC} (V)	+25°C			–40° to +85°C		–55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
HIGH Level Input Voltage	V_{IH}		2.0	1.5	–	–	1.5	–	1.5	–	V
			4.5	3.15	–	–	3.15	–	3.15	–	V
			6.0	4.2	–	–	4.2	–	4.2	–	V
LOW Level Input Voltage	V_{IL}		2.0	–	–	0.5	–	0.5	–	0.5	V
			4.5	–	–	1.35	–	1.35	–	1.35	V
			6.0	–	–	1.8	–	1.8	–	1.8	V
HIGH Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}, I_O = –0.02mA	2.0	1.9	–	–	1.9	–	1.9	–	V
			4.5	4.4	–	–	4.4	–	4.4	–	V
			6.0	5.9	–	–	5.9	–	5.9	–	V
		V_{IN} = V_{IH} or V_{IL}, I_O = –4mA	4.5	3.98	–	–	3.84	–	3.7	–	V
		V_{IN} = V_{IH} or V_{IL}, I_O = –5.2mA	6.0	5.48	–	–	5.34	–	5.2	–	V
LOW Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}, I_O = 0.02mA	2.0	–	–	0.1	–	0.1	–	0.1	V
			4.5	–	–	0.1	–	0.1	–	0.1	V
			6.0	–	–	0.1	–	0.1	–	0.1	V
		V_{IN} = V_{IH} or V_{IL}, I_O = 4mA	4.5	–	–	0.26	–	0.33	–	0.4	V
		V_{IN} = V_{IH} or V_{IL}, I_O = 5.2mA	6.0	–	–	0.26	–	0.33	–	0.4	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND	6.0	–	–	±0.1	–	±1.0	–	±1.0	μA
Quiescent Device Current	I_{CC}	V_{IN} = V_{CC} or GND, I_O = 0μA	6.0	–	–	8.0		80	–	160	μA

AC Electrical Characteristics: (t_r = t_f = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			–40° to +85°C		–55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Propagation Delay Address to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	175	–	220	–	265	ns
			4.5	–	–	35	–	44	–	53	ns
		C_L = 15pF	5.0	–	14	–	–	–	–	–	ns
		C_L = 50pF	6.0	–	–	30	–	37	–	45	ns

AC Electrical Characteristics (Cont'd): ($t_r = t_f$ = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			−40° to +85°C		−55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Propagation Delay $\overline{E1}$ to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	175	–	220	–	265	ns
			4.5	–	–	35	–	44	–	53	ns
		C_L = 15pF	5.0	–	14	–	–	–	–	–	ns
		C_L = 50pF	6.0	–	–	30	–	37	–	45	ns
Propagation Delay $\overline{E2}$ to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	175	–	220	–	265	ns
			4.5	–	–	35	–	44	–	53	ns
		C_L = 15pF	5.0	–	14	–	–	–	–	–	ns
		C_L = 50pF	6.0	–	–	30	–	37	–	45	ns
Output Transition Time	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	75	–	95	–	110	ns
			4.5	–	–	15	–	19	–	22	ns
			6.0	–	–	13	–	16	–	19	ns
Input Capacitance	C_{IN}		–	–	–	10	–	10	–	10	pF
Power Dissipation Capacitance	C_{PD}	Note 4, Note 5	5.0	–	88	–	–	–	–	–	pF

Note 4. C_{PD} is used to determine the dynamic power consumption, per gate.

Note 5. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Truth Table:

Inputs						Outputs															
E1	E2	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Level, L = LOW Level, X = Don't Care

Pin Connection Diagram