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NTE74LS181
Integrated Circuit
TTL – Arithmetic Logic Unit/Function Generator

Description:

The NTE74LS181 is an arithmetic logic unit (ALU)/function generator in a 24–Lead DIP type package that has the complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4–bit words as shown in Tables 1 and 2. These operations are selected by the four function–select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low–level voltage to the mode control input ((M). A full carry look–ahead scheme is made available in this device for fast, simultaneous carry generation by means of two cascade–outputs (Pin15 and Pin17) for the four bits in the package. When used in conjunction with the NTE74182 or NTE74S182, full carry look–ahead circuits, high–speed arithmetic operations can be performed. The typical addition times shown in the Typical Additional Times table illustrate the little additional time required for addition of longer words when full carry look–ahead is employed.

If high speed is not of importance, a ripple–carry input (C_n) and a ripple–carry output (C_{n+4}) are available. However, the ripple–carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

Features:

- Full Look–Ahead for High Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission–Line Effects
- Darlington Outputs Reduce Turn–Off Time
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive–OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logic Operations

Absolute Maximum Ratings: (T_A = 0° to +70°C unless otherwise specified)

Supply Voltage (Note 1), V_{CC} 7V
Input Voltage, V_I 5.5V
Interemitter Voltage (Note 2) 5.5V
Operating Ambient Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

Note 2. This is the voltage between two emitters of a multiple–emitter transistor. For this circuit, this rating applies to each $\overline{A}$ input in conjunction with inputs S2 or S3, and to each $\overline{B}$ input in conjunction with inputs S0 or S3.

Recommended Operation Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current (All outputs except A = B)	I_{OH}	–	–	−400	μA
Low−Level Output Current	I_{OL}	–	–	8	mA
Operating Ambient Temperature	T_A	0	–	70	°C

Electrical Characteristics: (T_A = 0° to +70°C, Note 3, Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}			2	–	–	V
Low−Level Input Voltage	V_{IL}			–	–	0.8	V
Low−Level Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	–	−1.5	V
High−Level Output Voltage Any Output Except A = B	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = −400μA		2.4	3.4	–	V
High−Level Output Current A = B Output Only	I_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, V_{OH} = 5.5V		–	–	100	μA
Low−Level Output Voltage All Outputs	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Output $\overline{G}$			I_{OL} = 16mA	–	0.47	0.7	V
Output $\overline{P}$			I_{OL} = 8mA	–	0.35	0.5	V
Input Current at Max Input Voltage Mode Input	I_I	V_{CC} = MAX, V_I = 5.5V		–	–	0.1	mA
Any $\overline{A}$ or $\overline{B}$ Input				–	–	0.3	mA
Any S Input				–	–	0.4	mA
Carry Input				–	–	0.5	mA
High−Level Input Current Mode Input	I_{IH}	V_{CC} = MAX, V_I = 2.7V		–	–	20	μA
Any $\overline{A}$ or $\overline{B}$ Input				–	–	60	μA
Any S Input				–	–	80	μA
Carry Input				–	–	100	μA
Low−Level Input Current Mode Input	I_{IL}	V_{CC} = MAX, V_I = 0.4V		–	–	−0.4	mA
Any $\overline{A}$ or $\overline{B}$ Input				–	–	−1.2	mA
Any S Input				–	–	−1.6	mA
Carry Input				–	–	−2.0	mA
Short−Circuit Output Current Any Output Except A = B	I_{OS}	V_{CC} = MAX, Note 5		−5	–	−42	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5	Condition A	–	20	34	mA
			Condition B	–	21	37	mA

Note 3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Note 4. All typical values at V_{CC} = 5V, T_A = +25°C.

Note 5. Not more than one output should be shorted at a time.

Note 6. With outputs open, I_{CC} is measured for the following conditions:

A. S0 through S3, M, and $\overline{A}$ inputs are at 4.5V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5V, all other inputs are grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C, C_L = 15pF, R_L = 2kΩ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From C_n Input to C_{n+4} Output)	t_{PLH}		–	18	27	ns
	t_{PHL}		–	13	20	ns
Propagation Delay Time (From Any $\overline{A}$ or $\overline{B}$ Input to C_{n+4} Output)	t_{PLH}	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	–	25	38	ns
	t_{PHL}		–	25	38	ns
Propagation Delay Time (From Any $\overline{A}$ or $\overline{B}$ Input to C_{n+4} Output)	t_{PLH}	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	–	27	41	ns
	t_{PHL}		–	27	41	ns
Propagation Delay Time (From C_n Input to Any $\overline{F}$ Output)	t_{PLH}	M = 0V, ($\overline{SUM}$ or $\overline{DIFF}$ Mode)	–	17	26	ns
	t_{PHL}		–	13	20	ns
Propagation Delay Time (From Any $\overline{A}$ or $\overline{B}$ Input to $\overline{G}$ Output)	t_{PLH}	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	–	19	29	ns
	t_{PHL}		–	15	23	ns
Propagation Delay Time (From Any $\overline{A}$ or $\overline{B}$ Input to $\overline{G}$ Output)	t_{PLH}	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	–	21	32	ns
	t_{PHL}		–	21	32	ns
Propagation Delay Time (From Any $\overline{A}$ or $\overline{B}$ Input to $\overline{P}$ Output)	t_{PLH}	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	–	20	30	ns
	t_{PHL}		–	20	30	ns
Propagation Delay Time (From Any $\overline{A}$ or $\overline{B}$ Input to $\overline{P}$ Output)	t_{PLH}	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	–	20	30	ns
	t_{PHL}		–	22	33	ns
Propagation Delay Time (From Any $\overline{A}_i$ or $\overline{B}_i$ Input to $\overline{F}_i$ Output)	t_{PLH}	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	–	21	32	ns
	t_{PHL}		–	13	20	ns
Propagation Delay Time (From Any $\overline{A}_i$ or $\overline{B}_i$ Input to $\overline{F}_i$ Output)	t_{PLH}	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	–	21	32	ns
	t_{PHL}		–	21	32	ns
Propagation Delay Time (From Any $\overline{A}_i$ or $\overline{B}_i$ Input to $\overline{F}_i$ Output)	t_{PLH}	M = 4.5V (Logic Mode)	–	22	33	ns
	t_{PHL}		–	26	38	ns
Propagation Delay Time (From Any $\overline{A}$ or $\overline{B}$ Input to A = B Output)	t_{PLH}	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	–	33	50	ns
	t_{PHL}		–	41	62	ns

Typical Addition Times:

Number of Bits	Additional Times Using ’LS181 and ’182	Package Count: Arithmetic/ Logic Units	Package Count: Look–Ahead Carry Generators	Carry Method Between ALU’s
1 to 4	24ns	1	–	None
5 to 8	40ns	2	–	Ripple
9 to 16	44ns	3 or 4	1	Full Look–Ahead
17 to 64	68ns	5 to 16	2 to 5	Full Look–Ahead

Description (Cont’d):

The NTE74LS181 will accommodate active–high or active–low data if the pin designations are interpreted as follows:

Pin Number	2	1	23	22	21	21	19	18	9	10	11	13	7	16	15	17
Active–Low Data (Table 1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active–High Data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Description (Cont'd):

Subtraction is accomplished by 1's complement addition where the 1's complement of the substrahend is generated internally. The resultant output is A−B−1, which requires an end−around or forced carry to provide A−B.

The NTE74LS181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and b inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open−collector so that it can be wire−AND connected to give a comparison fo more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	Active−Low Data	Active−High Data
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

This circuit has been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function−select inputs (S0, S1, S2, S3) with the mode−control input (M) at a high level to disable th internal carry. The 16 logic functions are detailed in tables 1 and 2 and include exclusive−OR, NAND, AND, NOR, and OR functions.

Signal Designations:

The NTE74LS181 together with the '182 and 'S182 can be used with the signal designations of either Figure 1 or Figure 2. The inversion indicators (O) and the bars over the terminal letter symbols (e.g., $\overline{C}$) each indicate that the associated input or output is active with respect to the selected function of the device when the input output is low. That is, a low $\overline{C}$ means "do carry" while a high means "do not carry".

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

Figure 1:

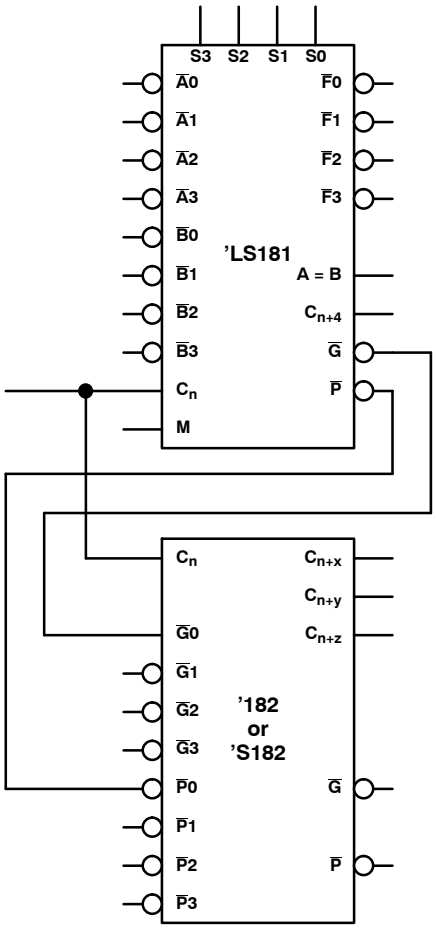

Table 1:

Selection				Active–Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

Figure 2:

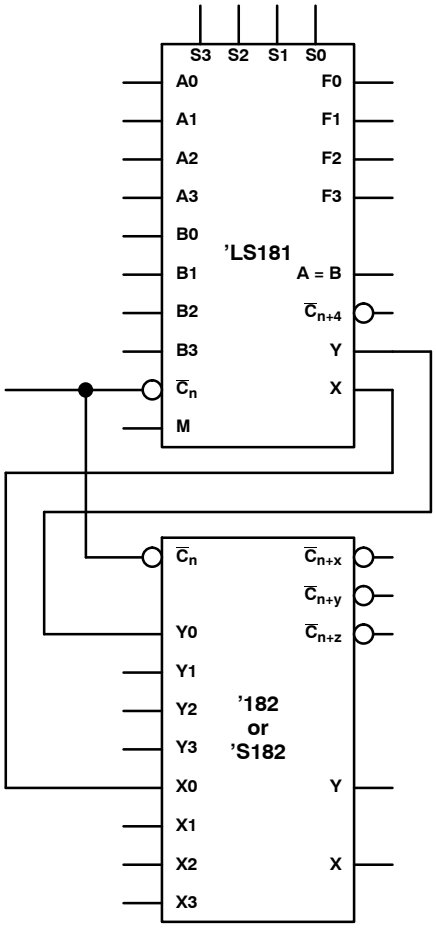

Table 2:

Selection				Active–High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + $\overline{B}$) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

Parameter Measurement Information:

$\overline{\text{SUM}}$ Mode Test Table

Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	F_i	In−Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	F_i	In−Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In−Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In−Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In−Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In−Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In−Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out−of−Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out−of−Phase
t_{PHL}							

$\overline{\text{DIFF}}$ Mode Test Table

Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	In−Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	F_i	Out−of−Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In−Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out−of−Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In−Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out−of−Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In−Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out−of−Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or Any $\overline{F}$	In−Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out−of−Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In−Phase
t_{PHL}							

Parameter Measurement Information (Cont'd):

Logic Mode Test Table

Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	F_i	Out–of–Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	F_i	Out–of–Phase
t_{PHL}							

Pin Connection Diagram: