SNx4HC02 Quadruple 2-Input Positive-NOR Gates

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption: Maximum I_{CC} of 20 µA
- Typical t_{pd} = 8 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1-µA Maximum

2 Applications

- Education
- Toys
- Musical Instruments
- Medical Healthcare and Fitness
- Grid Infrastructure
- Electronic Point of Sale
- Test and Measurement
- Factory Automation and Control
- Building Automation
- RS Latch
- Falling Edge Detector

3 Description

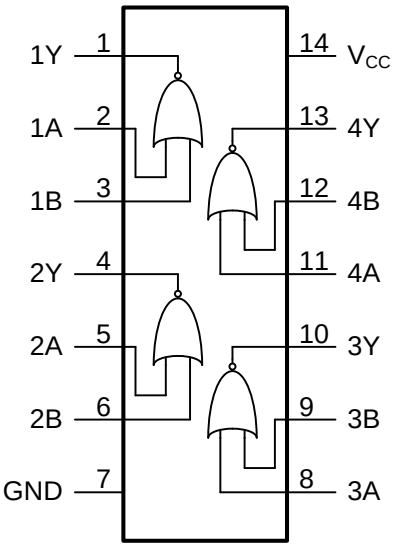
The SNx4HC02 devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC02D	SOIC (14)	4.90 mm × 3.91 mm
SN74HC02N	PDIP (14)	19.30 mm × 6.35 mm
SN74HC02PW	TSSOP (14)	5.00 mm × 4.40 mm
SN74HC02NS	SO (14)	10.30 mm × 5.30 mm
SN74HC02DB	SSOP (14)	6.20 mm × 5.30 mm
SN54HC02J	CDIP (14)	19.94 mm × 7.62 mm
SN54HC02W	CFP (14)	9.21 mm × 7.11 mm
SN54HC02FK	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SNx4HC02 Functional Block Diagram



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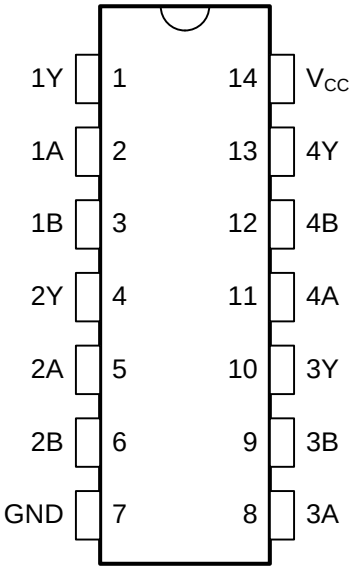
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

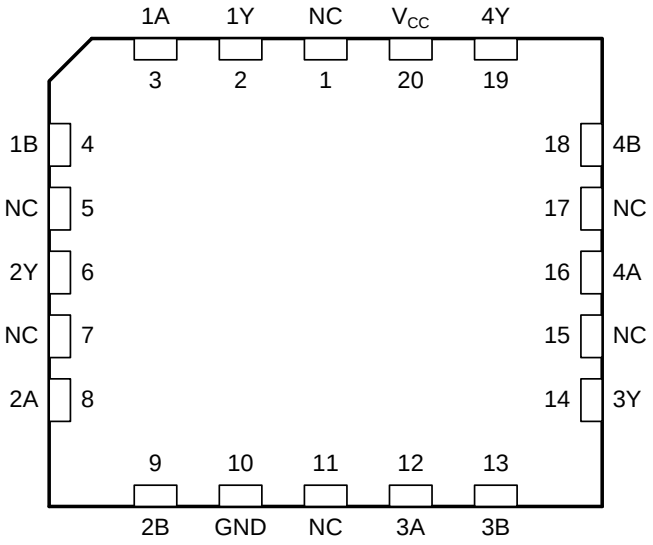
Changes from Revision E (August 2003) to Revision F	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Removed ordering information.	1

5 Pin Configuration and Functions

D, DB, N, NS, PW, J, or W Package
14-Pin SOIC, SSOP, PDIP, SO, TSSOP, CDIP, or CFP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, SSOP, PDIP, SO, TSSOP, CDIP, CFP	LCCC		
1Y	1	2	O	Gate 1 output
1A	2	3	I	Gate 1 input A
1B	3	4	I	Gate 1 input B
2Y	4	6	O	Gate 2 output
2A	5	8	I	Gate 2 input A
2B	6	9	I	Gate 2 input B
GND	7	10	—	Ground Pin
3A	8	12	I	Gate 3 input A
3B	9	13	I	Gate 3 input B
3Y	10	14	O	Gate 3 output
4A	11	16	I	Gate 4 input A
4B	12	18	I	Gate 4 input B
4Y	13	19	O	Gate 4 output
V_{CC}	14	20	—	Power pin
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_j	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings – SN74HC02

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1).

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2 V			1000	ns/V
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN54HC02	–55		125	°C
		SN74HC02	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information – SN74HC02

THERMAL METRIC[1]		SN74HC02					UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	94	105.4	54.9	88.8	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.2	57.3	42.5	46.5	48.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.7	52.7	34.7	47.6	61.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.6	22.6	27.9	16.8	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.4	52.2	34.6	47.2	60.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information – SN54HC02

THERMAL METRIC[1]		SN54HC02			UNIT
		J (CDIP)	W (CFP)	FK (LCCC)	
		14 PINS	14 PINS	20 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.8	89.6	61.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.1	164.1	59.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	26.7	15.5	11.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A	MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V		1.9	1.998		V
			4.5 V		4.4	4.499		
			6 V		5.9	5.999		
		I_{OH} = –4 mA	4.5 V	T_A = 25°C	3.98	4.3		
				SN54HC02	3.7			
				SN74HC02	3.84			
		I_{OH} = –5.2 mA	6 V	T_A = 25°C	5.48	5.8		
				SN54HC02	5.2			
				SN74HC02	5.34			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V			0.002	0.1	V
			4.5 V			0.001	0.1	
			6 V			0.001	0.1	
		I_{OL} = 4 mA	4.5 V	T_A = 25°C		0.17	0.26	
				SN54HC02			0.4	
				SN74HC02			0.33	
		I_{OL} = 5.2 mA	6 V	T_A = 25°C		0.15	0.26	
				SN54HC02			0.4	
				SN74HC02			0.33	
I_I	$V_I = V_{CC}$ or 0		6 V	T_A = 25°C		±0.1	±100	nA
				SN54HC02, SN74HC02			±1000	
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V	T_A = 25°C			2	µA
				SN54HC02			40	
				SN74HC02			20	
C_i			2 V to 6 V			3	10	pF

6.7 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
t_{pd}	A or B	Y	2 V	T_A = 25°C		45	90	ns
				SN54HC02			135	
				SN74HC02			115	
			4.5 V	T_A = 25°C		9	18	
				SN54HC02			27	
				SN74HC02			23	
			6 V	T_A = 25°C		8	15	
				SN54HC02			23	
				SN74HC02			20	
t_t	A or B	Y	2 V	T_A = 25°C		38	75	ns
				SN54HC02			110	
				SN74HC02			95	
			4.5 V	T_A = 25°C		8	15	
				SN54HC02			22	
				SN74HC02			19	
			6 V	T_A = 25°C		6	13	
				SN54HC02			19	
				SN74HC02			16	

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	22	pF

6.9 Typical Characteristics

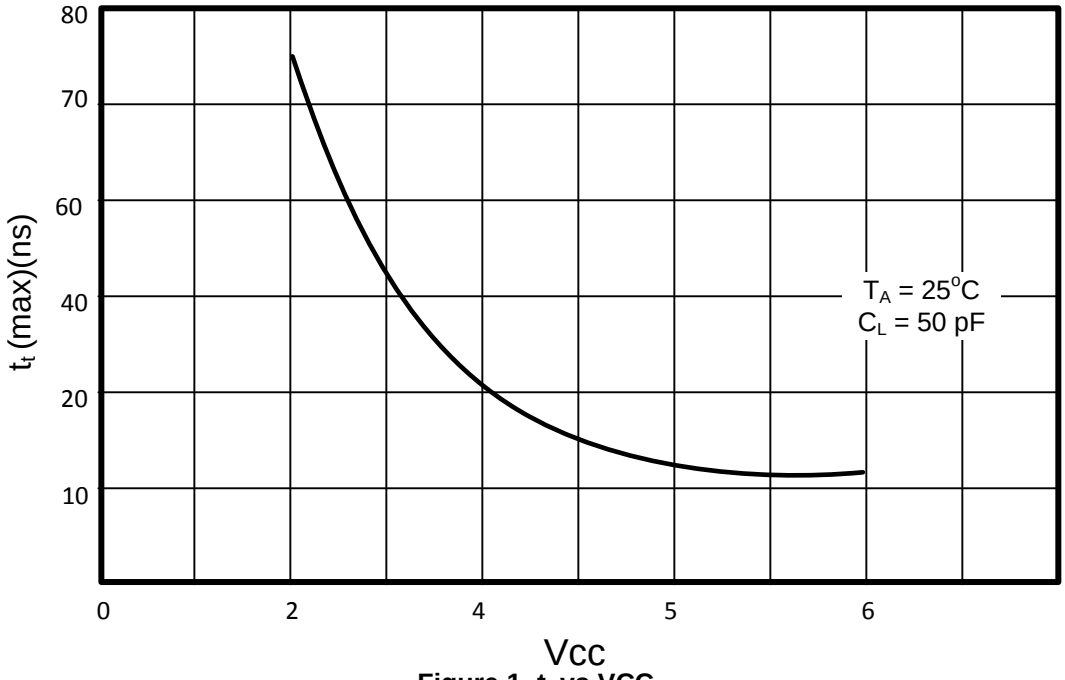
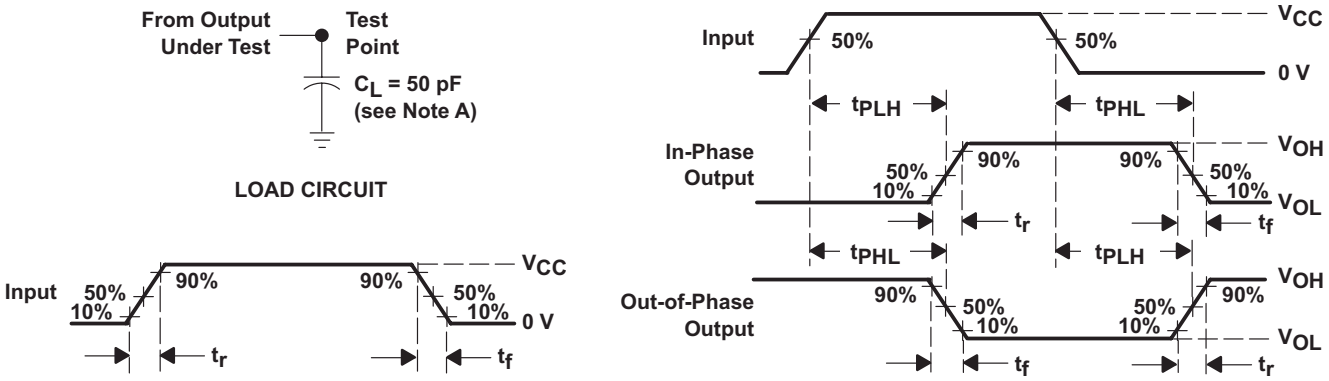


Figure 1. t_t vs VCC

7 Parameter Measurement Information



A. C_L includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

C. The outputs are measured one at a time with one input transition per measurement.

D. t_{PLH} and t_{PHL} are the same as t_{pd}.

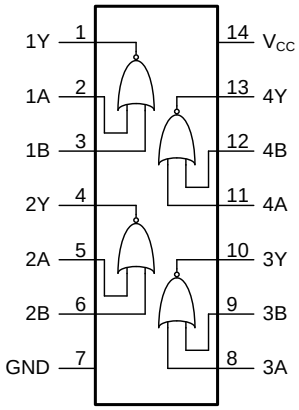
Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4HC02 devices are quad 2-input NOR gates. These devices are members of the High-Speed CMOS (HC) logic family. The HC family of logic is optimized to operate with a 5-V supply, is low noise without characteristic overshoot and undershoot, has low power consumption, small propagation delay, balanced propagation delay and transition times, and operates over a wide temperature range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage Range

The SNx4HC series of devices offer a wide operating voltage range from 2 V to 6 V.

8.3.2 LSTTL Loads

The outputs of the SNx4HC series can drive up to 10 LSTTL loads.

8.3.3 Low Power Consumption

The SNx4HC02 offers low power consumption of 20 µA maximum.

8.3.4 Output Drive Capability

At 5 V, the outputs have ±4 mA of output drive capability.

8.3.5 Low Input Current Leakage

Inputs have low input current leakage of 1 µA maximum.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4HC02.

Table 1. Function Table

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

Figure 3. Logic Diagram (Positive Logic)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNX4HC02 is a low-drive CMOS device that can be used for a multitude of NOR type functions. The device can produce 4 mA of drive current at 5 V, making it Ideal for driving multiple outputs and good for low-noise applications. This application is for using a single SNX4HC02 as a falling edge detector circuit.

The edge detector operates by using the inherent propagation delay from input to output of each device stage. In steady-state, the inputs to the output stage will always be different, and thus the output will always be low. Only during the brief time when both inputs are low (that is, immediately following a falling edge on V_{IN}), the output will be high.

9.2 Typical Application

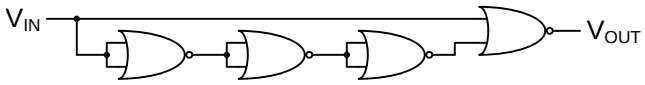


Figure 4. Falling Edge Detector Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

The output pulse time will be approximately three times t_{pd} from *Switching Characteristics* for the selected V_{CC}, device, and temperature range.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions – For rise time and fall time specifications, see Δt/ΔV in *Recommended Operating Conditions*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   - Inputs are not overvoltage tolerant, allowing them to go as high as V_{CC}.
2. Recommend Output Conditions
   - Load currents must not exceed 20 mA per output and 50 mA total for the part.
   - Outputs must not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curve

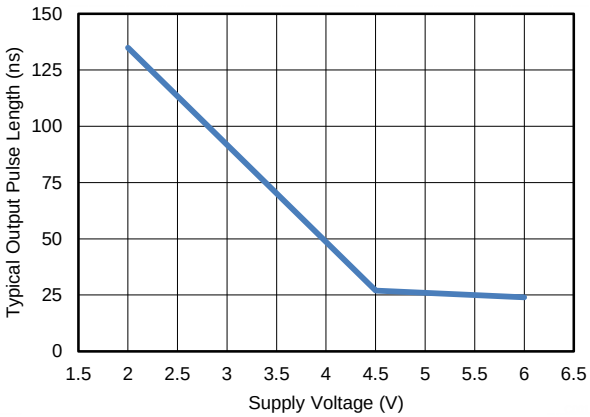


Figure 5. Typical Output Pulse Length Over V_{CC} Range

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*. Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF bypass capacitor. If there are multiple V_{CC} pins, TI recommends a 0.01-μF or 0.022-μF bypass capacitors for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. Two bypass capacitors of value 0.1 μF and 1 μF are commonly used in parallel. For best results, install the bypass capacitor(s) as close to the power pin as possible.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in *Absolute Maximum Ratings* are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

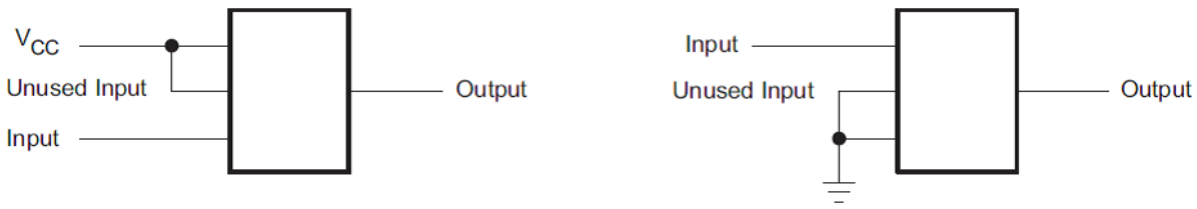


Figure 6. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC02	Click here	Click here	Click here	Click here	Click here
SN74HC02	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)
5962-8404101VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8404101VC A SNV54HC02J
84041012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84041012A SNJ54HC 02FK
8404101CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404101CA SNJ54HC02J
8404101DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404101DA SNJ54HC02W
JM38510/65101B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 65101B2A
JM38510/65101BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65101BCA
JM38510/65101BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65101BDA
M38510/65101B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 65101B2A
M38510/65101BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65101BCA
M38510/65101BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65101BDA
SN54HC02J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC02J
SN74HC02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC02

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)
SN74HC02DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU | CU SN	N / A for Pkg Type	-40 to 85	SN74HC02N
SN74HC02NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC02N
SN74HC02NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SN74HC02PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC02
SNJ54HC02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84041012A SNJ54HC 02FK
SNJ54HC02J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404101CA SNJ54HC02J
SNJ54HC02W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404101DA SNJ54HC02W

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54HC02, SN54HC02-SP, SN74HC02 :

- Catalog: SN74HC02, SN54HC02
- Automotive: SN74HC02-Q1, SN74HC02-Q1
- Enhanced Product: SN74HC02-EP, SN74HC02-EP

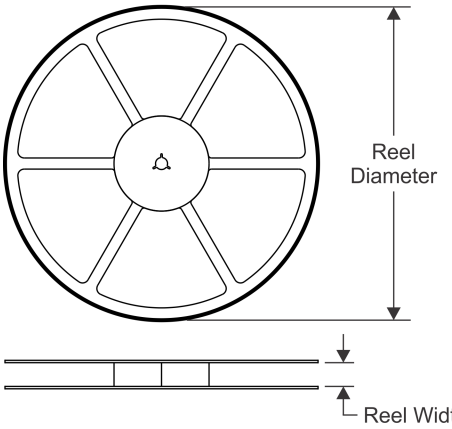
- Military: SN54HC02
- Space: SN54HC02-SP

NOTE: Qualified Version Definitions:

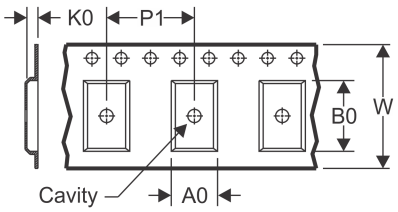
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

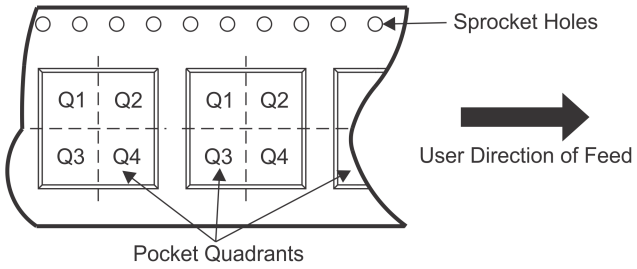


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

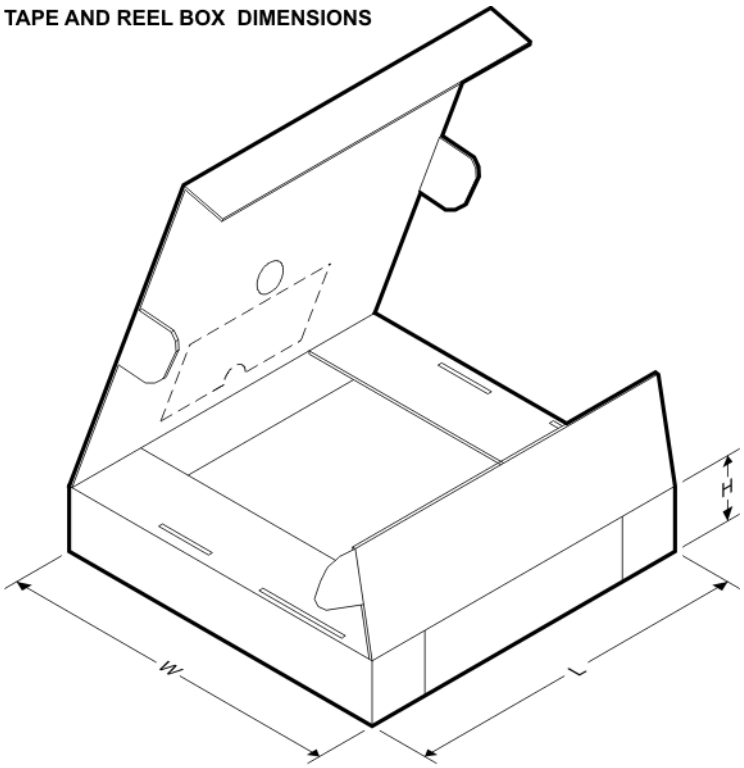
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC02DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC02DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC02DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC02DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC02DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC02DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC02DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC02PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC02PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC02PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC02PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

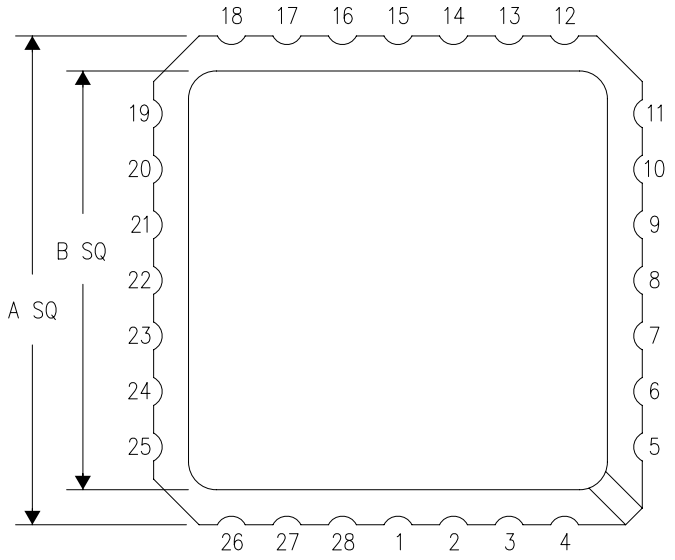


*All dimensions are nominal

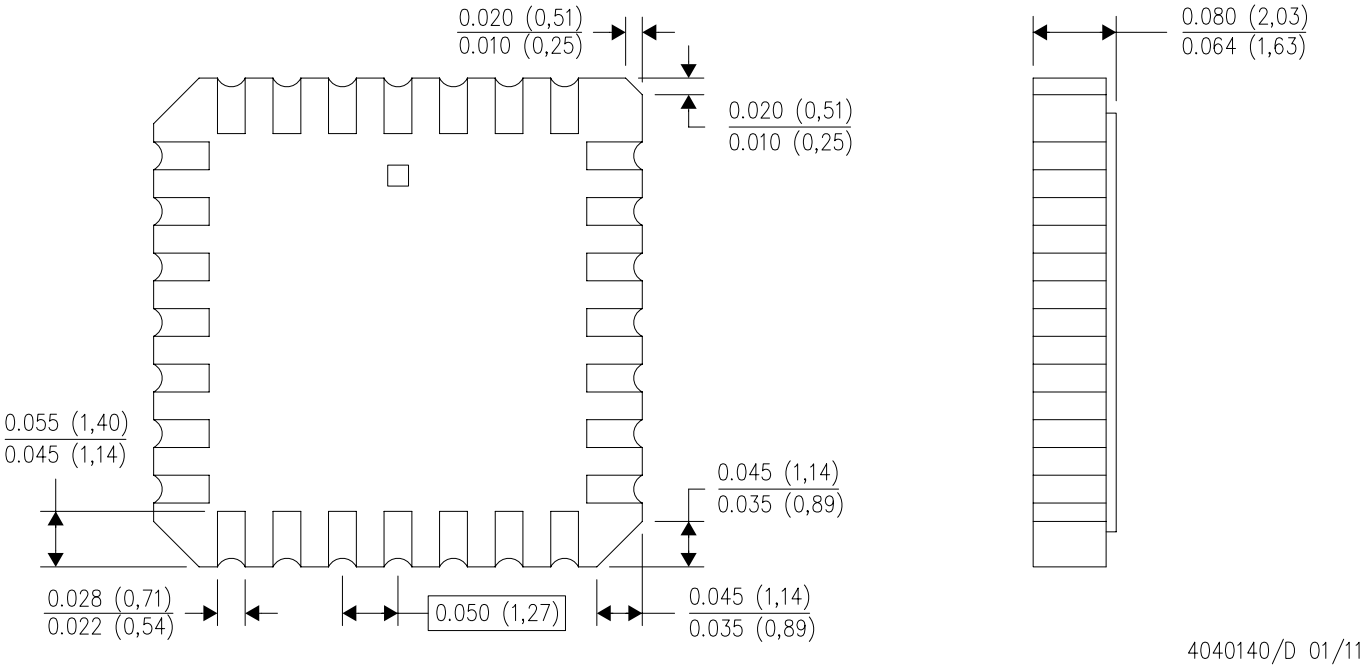
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC02DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74HC02DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC02DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC02DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC02DRG4	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC02DRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC02DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC02PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74HC02PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC02PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC02PWT	TSSOP	PW	14	250	367.0	367.0	35.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



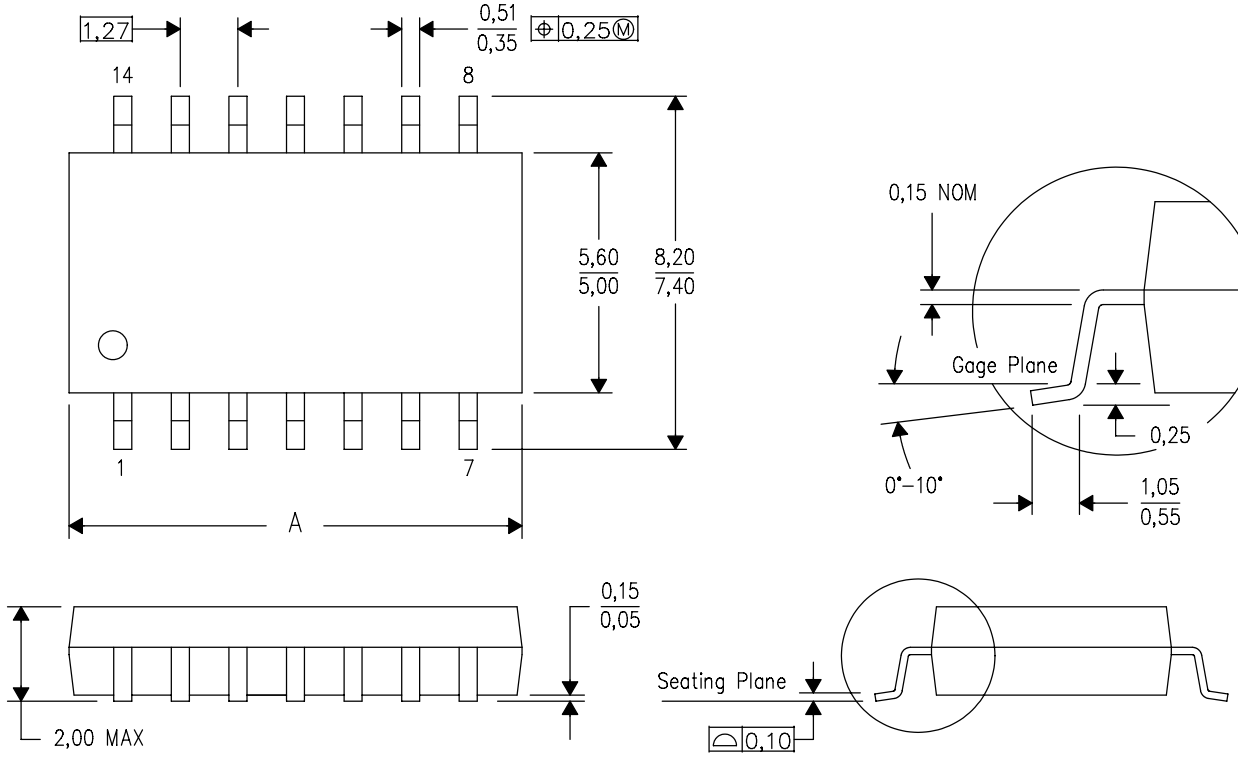
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

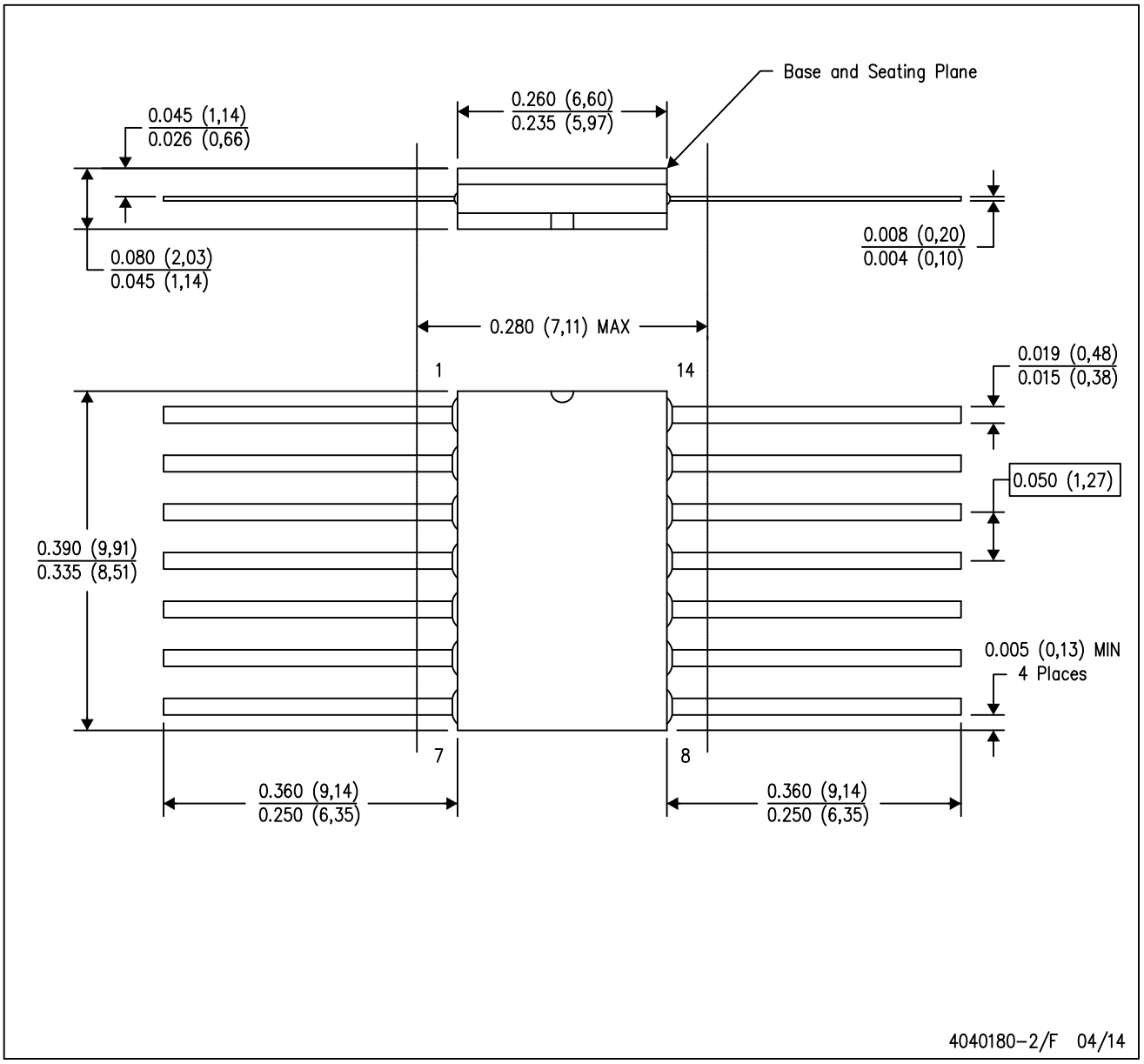


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

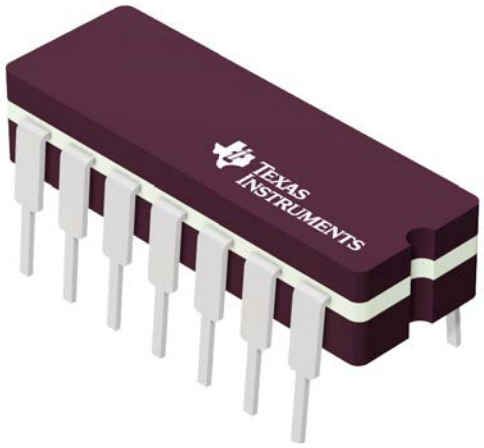


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

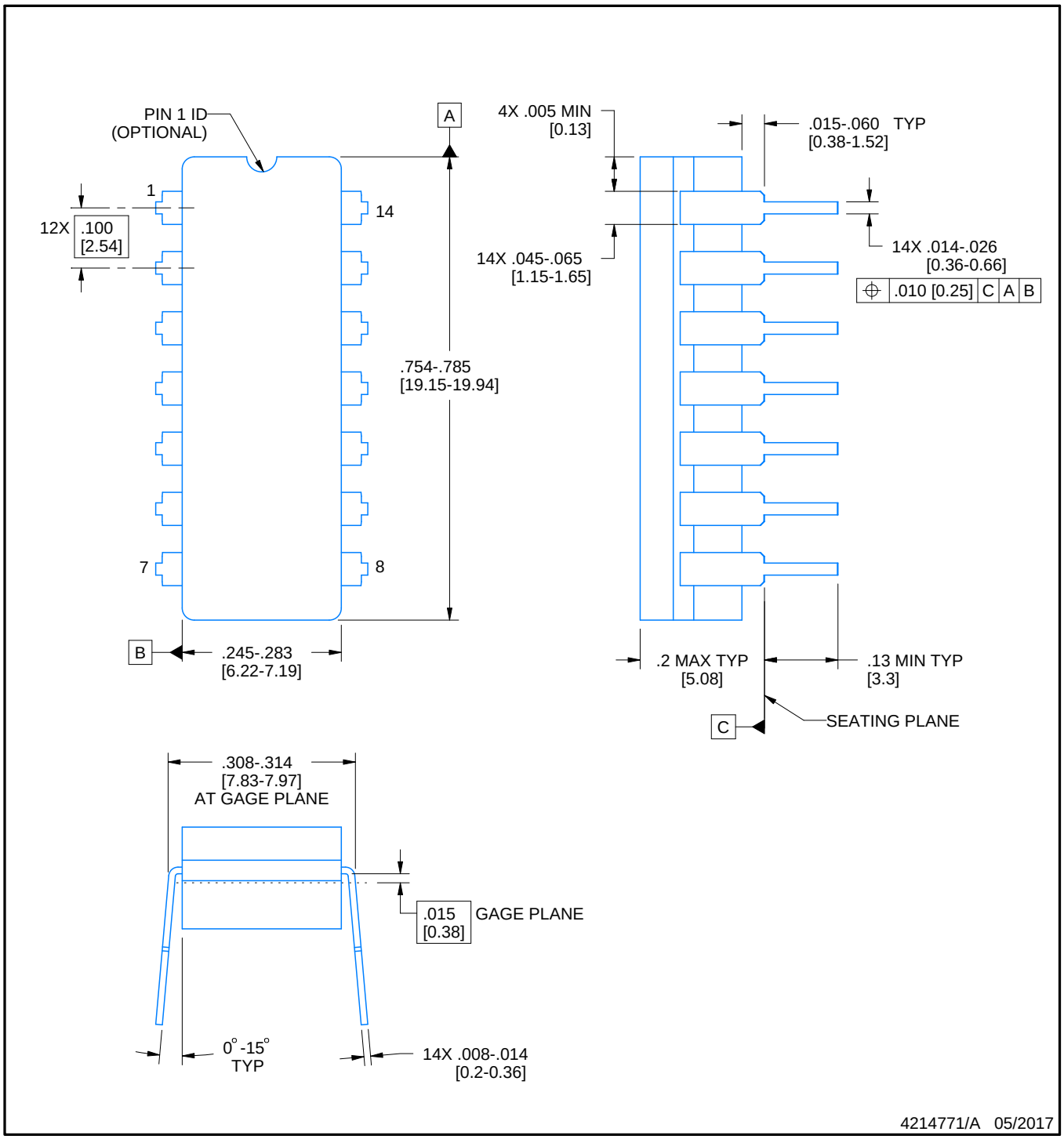
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

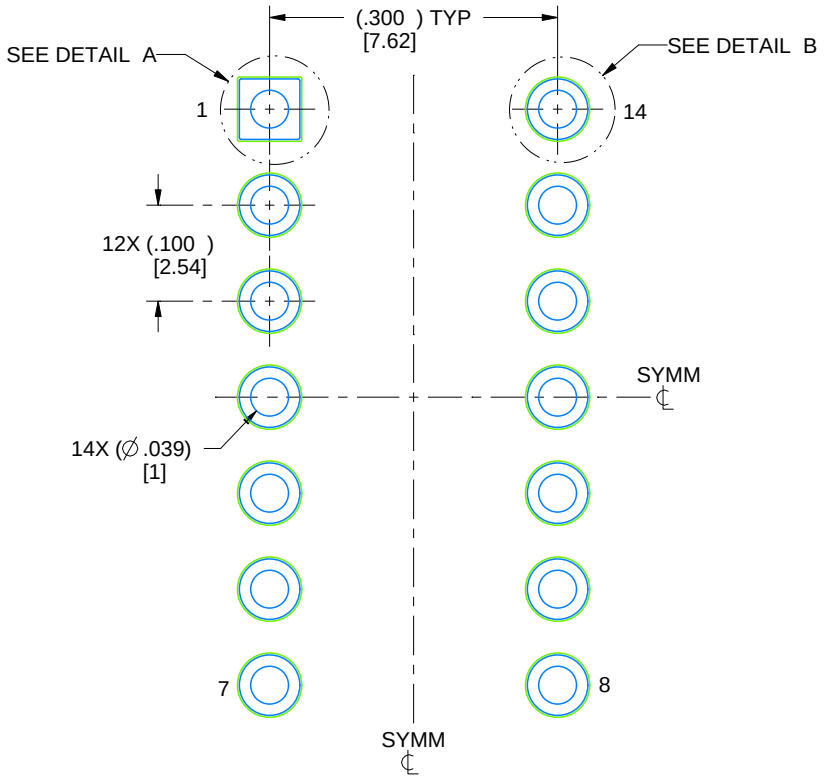
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

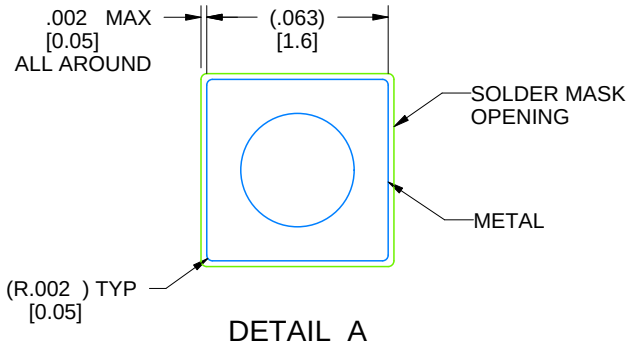
J0014A

CDIP - 5.08 mm max height

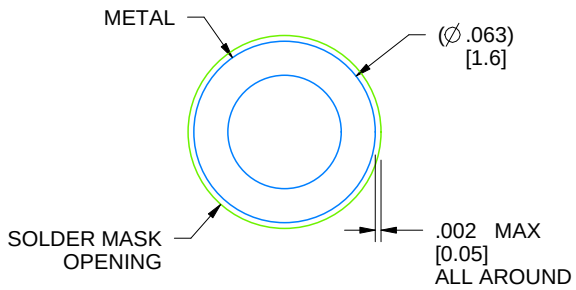
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



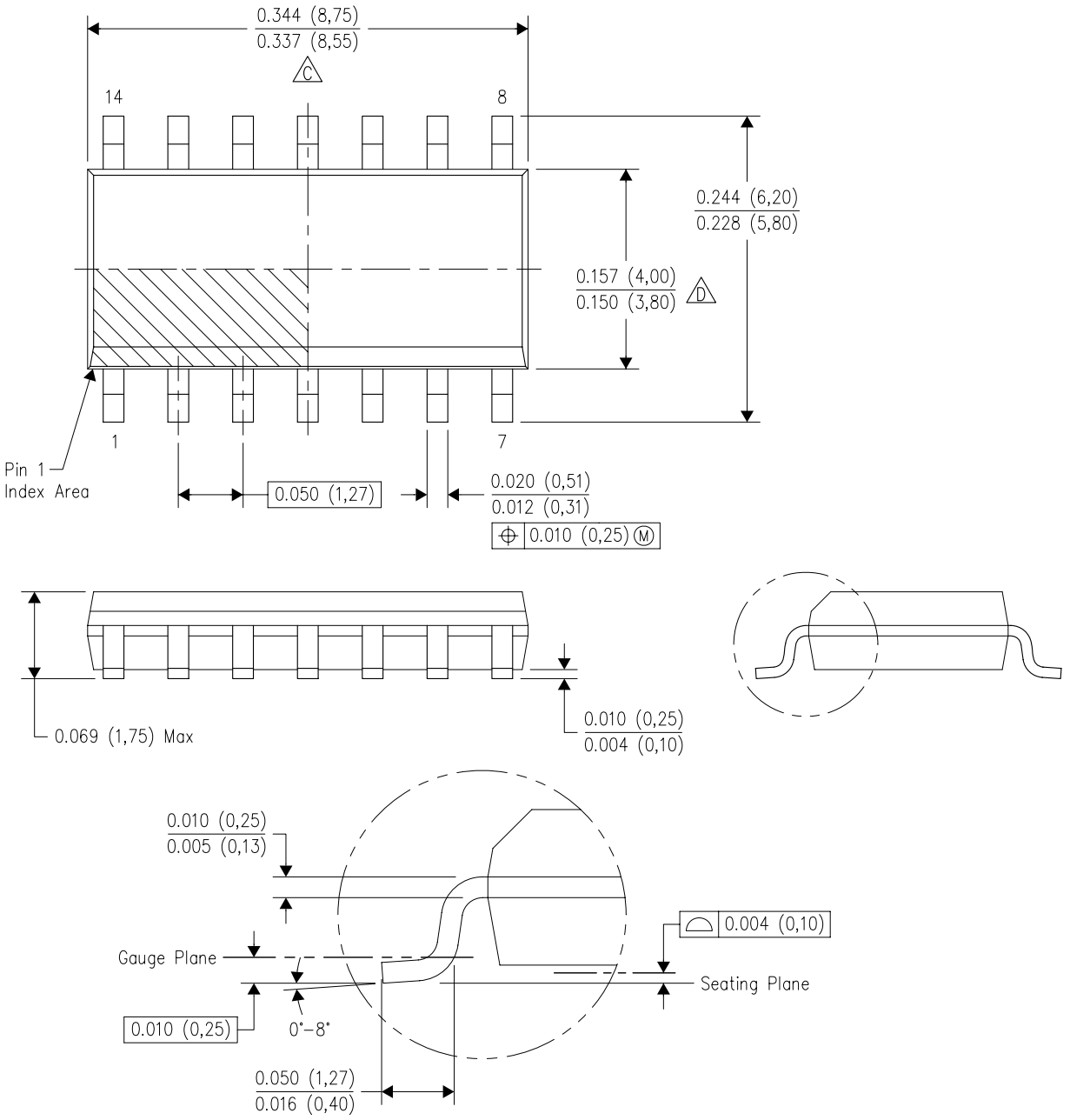
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

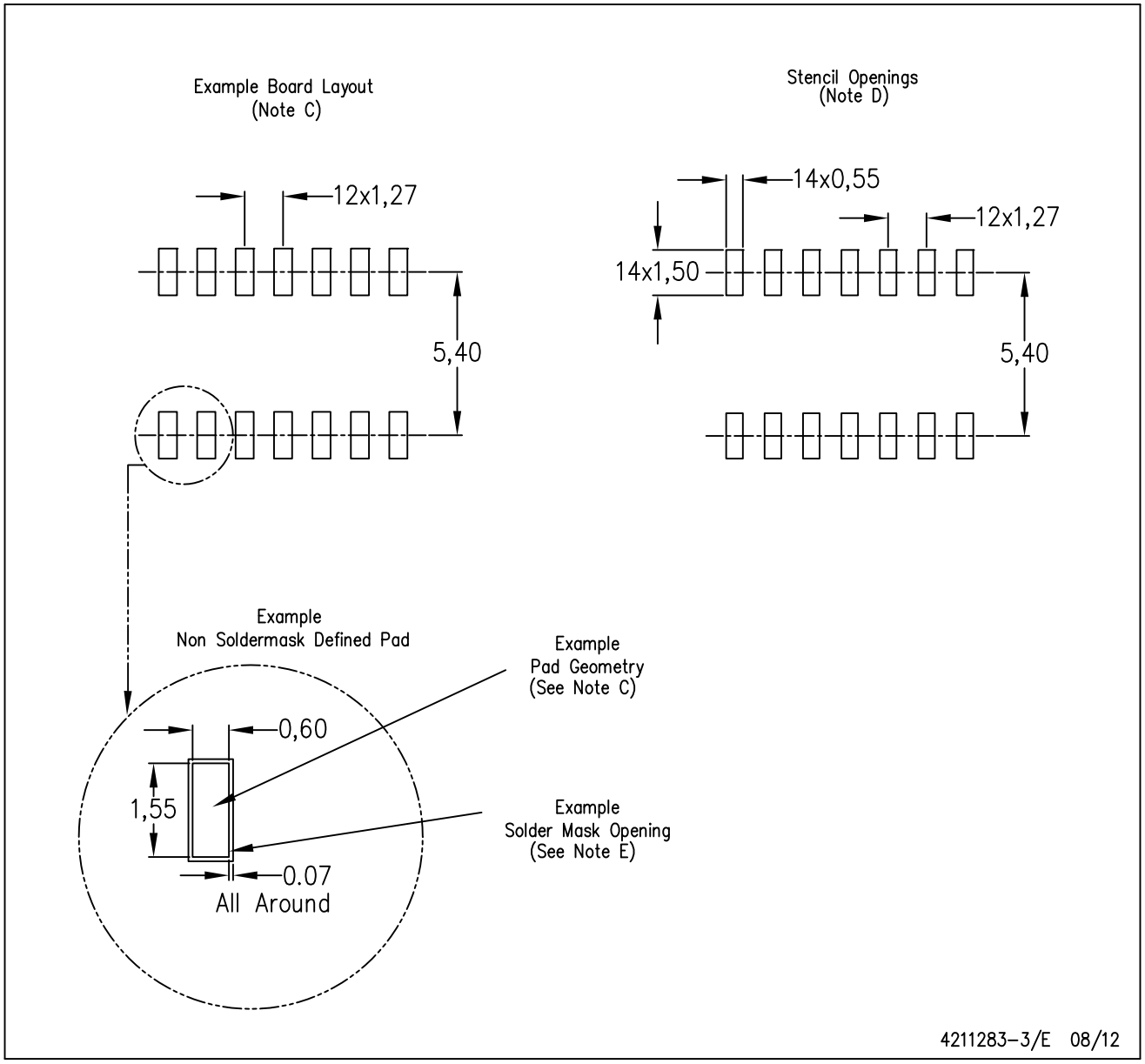
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

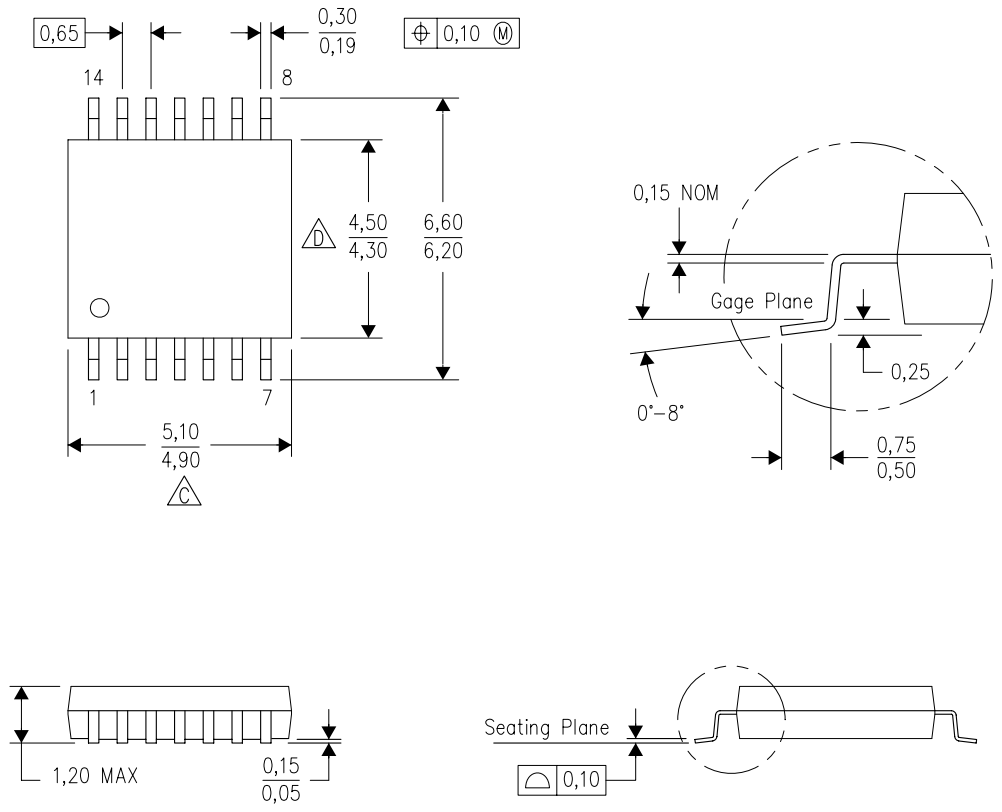
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

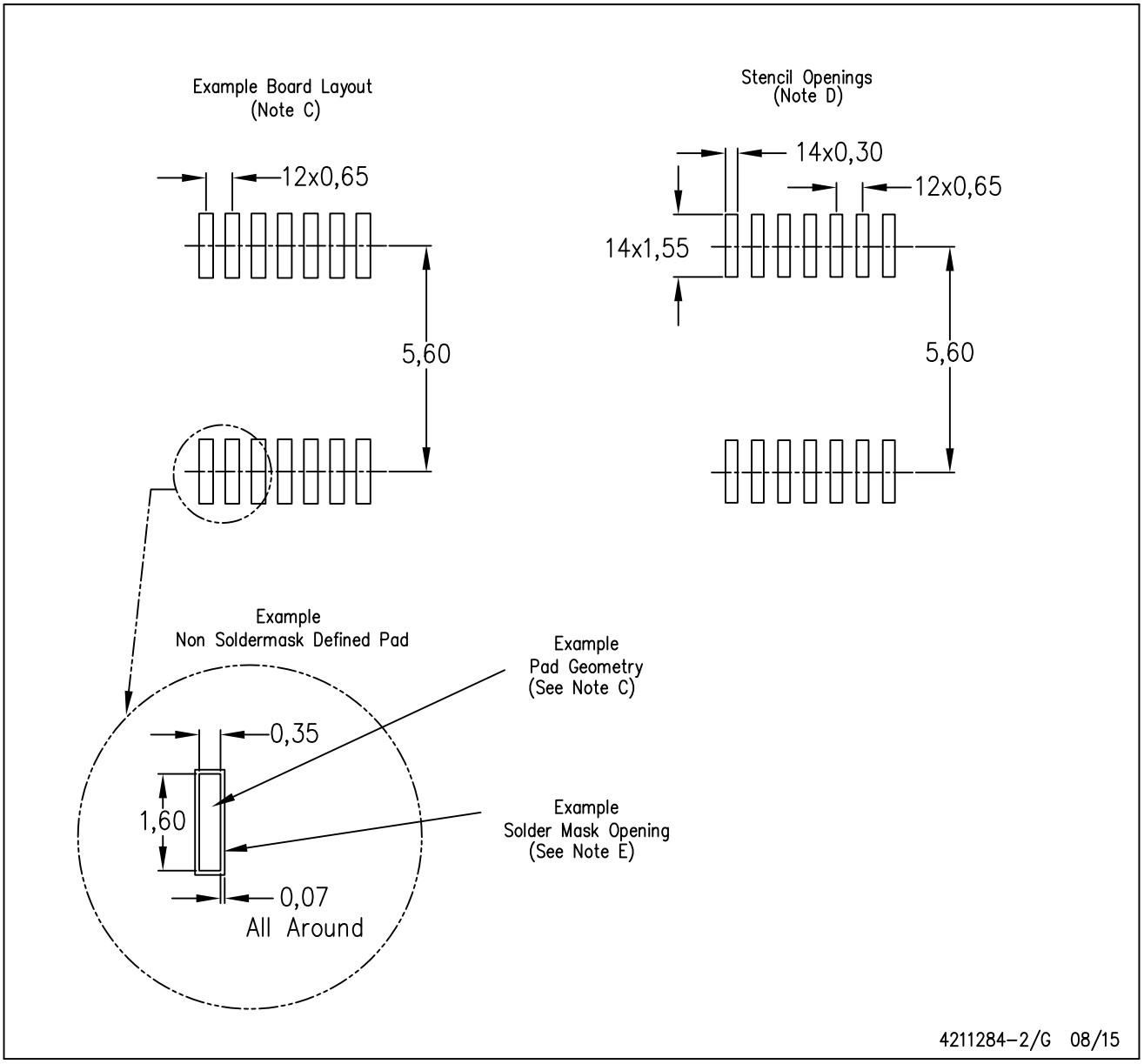
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

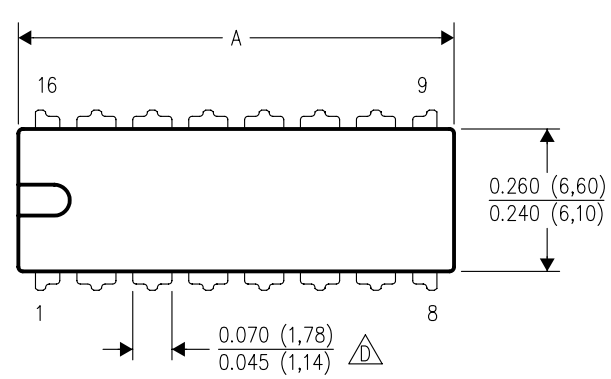


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

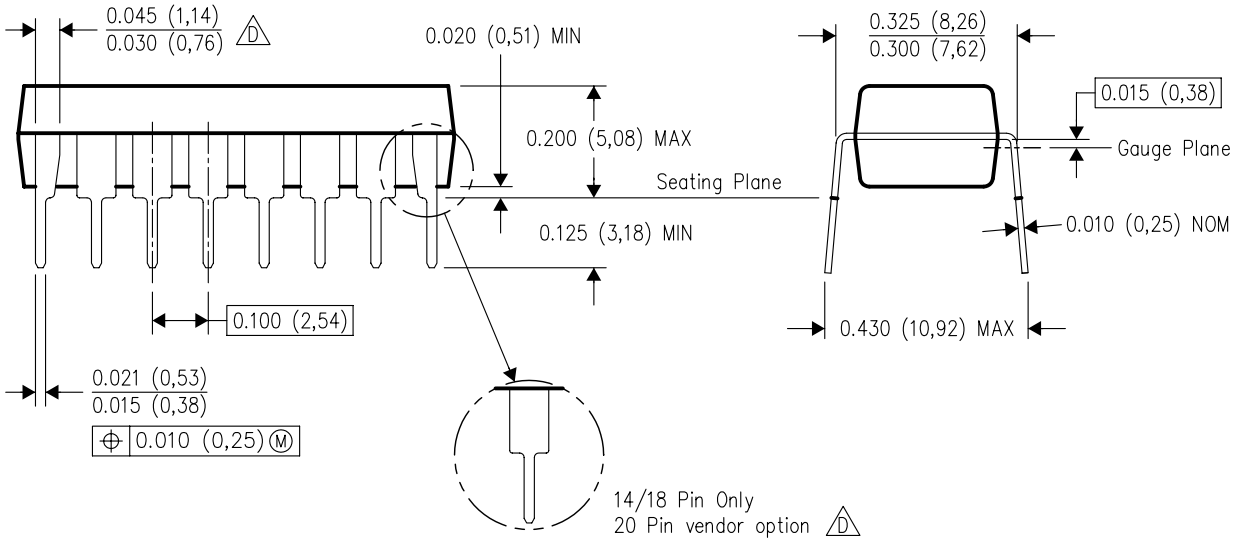
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



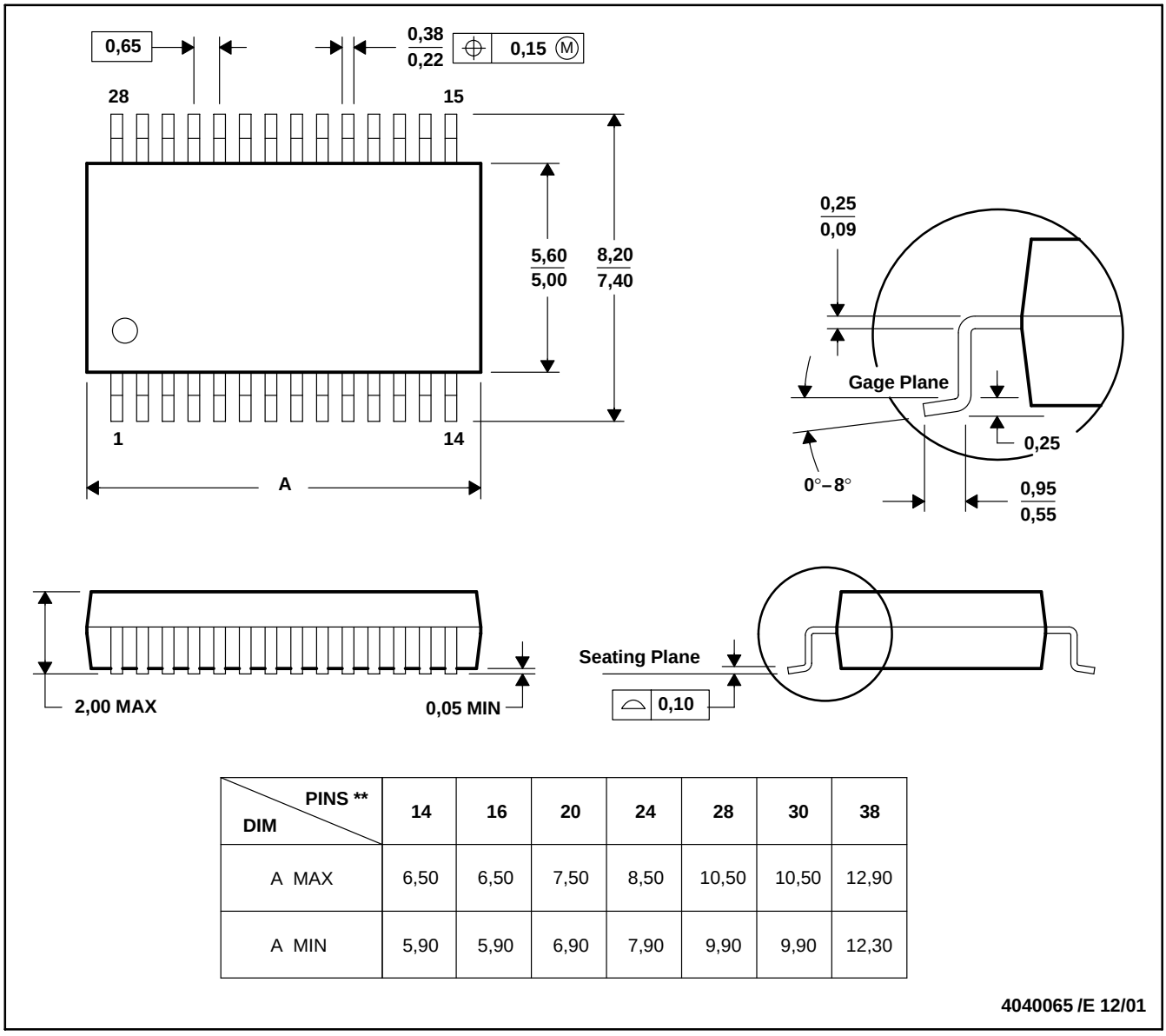
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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