SN754410 Quadruple Half-H Driver

1 Features

- 1-A Output-Current Capability Per Driver
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- Designed for Positive-Supply Applications
- Wide Supply-Voltage Range of 4.5 V to 36 V
- TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- Input Hysteresis Improves Noise Immunity
- 3-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- No Output Glitch During Power Up or Power Down
- Improved Functional Replacement for the SGS L293

2 Applications

- Stepper Motor Drivers
- DC Motor Drivers
- Latching Relay Drivers

3 Description

The SN754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents up to 1 A at voltages from 4.5 V to 36 V. The device is designed to drive inductive loads such as relays, solenoids, DC and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL-and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage V_{CC2} is used for the output circuits.

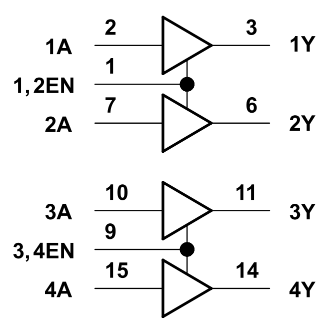
The SN754410 is designed for operation from −40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
SN754410	PDIP (16)	19.80 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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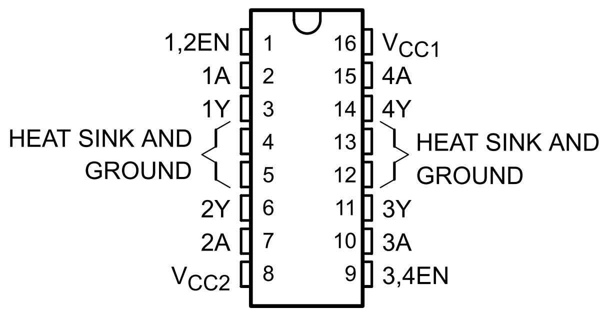
5 Revision History

Changes from Revision B (November 1995) to Revision C **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted *Ordering Information* table. 1

6 Pin Configuration and Functions

NE PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1,2EN	1	I	Enable driver channels 1 and 2 (active high input)
<1:4>A	2, 7, 10, 15	I	Driver inputs, non-inverting
<1:4>Y	3, 6, 11, 14	O	Driver outputs
GROUND	4, 5, 12, 13	—	Device ground and heat sink pin. Connect to circuit board ground plane with multiple solid vias
V_{CC2}	8	—	Power VCC for drivers 4.5V to 36V
3,4EN	9	I	Enable driver channels 3 and 4 (active high input)
V_{CC1}	16	—	5V supply for internal logic translation

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{CC1}	Output supply voltage range	–0.5	36	V
V_{CC2}	Output supply voltage range	–0.5	36	V
V_I	Input voltage	–0.5	36	V
V_O	Output voltage range	–3	V_{CC2} + 3	V
I_P	Peak output current		±2	A
I_O	Continuous output current		±1	A
P_D	Continuous total power dissipation at (or below) 25°C free-air temperature(3)		2075	mW
T_A	Operating free-air temperature range	–40	85	°C
T_J	Operating virtual junction temperature range	–40	150	°C
T_{stg}	Storage temperature range		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND.
(3) For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC1}	Logic supply voltage	4.5	5.5	V
V_{CC2}	Output supply voltage	4.5	36	V
V_{IH}	High-level input voltage	2	5.5	V
V_{IL}	Low-level input voltage	–0.3(1)	0.8	V
T_J	Operating virtual junction temperature	–40	125	°C
T_A	Operating free-air temperature	–40	85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

7.3 Thermal Information

THERMAL METRIC(1)		SN754410	UNIT
		NE	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –12 mA			–0.9	–1.5	V
V_{OH}	High-level output voltage	I_{OH} = –0.5 A		V_{CC2} – 1.5	V_{CC2} – 1.1		V
		I_{OH} = –1 A		V_{CC2} – 2			
		I_{OH} = –1 A, T_J = 25°C		V_{CC2} – 1.8	V_{CC2} – 1.4		
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A			1	1.4	V
		I_{OL} = 1 A				2	
		I_{OL} = 1 A, T_J = 25°C			1.2	1.8	
V_{OKH}	High-level output clamp voltage	I_{OK} = –0.5 A			V_{CC2} + 1.4	V_{CC2} + 2	V
		I_{OK} = 1 A			V_{CC2} + 1.9	V_{CC2} + 2.5	
V_{OKL}	Low-level output clamp voltage	I_{OK} = 0.5 A			–1.1	–2	V
		I_{OK} = –1 A			–1.3	–2.5	
$I_{OZ(off)}$	Off-state high-impedance-state output current	V_O = V_{CC2}				500	µA
		V_O = 0				–500	
I_{IH}	High-level input current	V_I = 5.5 V				10	µA
I_{IL}	Low-level input current	V_I = 0				–10	µA
I_{CC1}	Output supply current	I_O = 0	All outputs at high level			38	mA
			All outputs at low level			70	
			all outputs at high impedance			25	
I_{CC2}	Output supply current	I_O = 0	All outputs at high level			33	nA
			All outputs at low level			20	
			All outputs at high impedance			5	

7.5 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), V_{CC1} = 5 V, V_{CC2} = 24 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time, high-to-low-level output from A input	See Figure 3		400		ns
t_{d2}	Delay time, low-to-high-level output from A input			800		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns
t_{en1}	Enable time to the high level	See Figure 4		700		ns
t_{en2}	Enable time to the low level			400		ns
t_{dis1}	Disable time from the high level			900		ns
t_{dis2}	Disable time from the low level			600		ns

7.6 Typical Characteristics

V_{CC1} = 5 V, V_{CC2} = 24 V

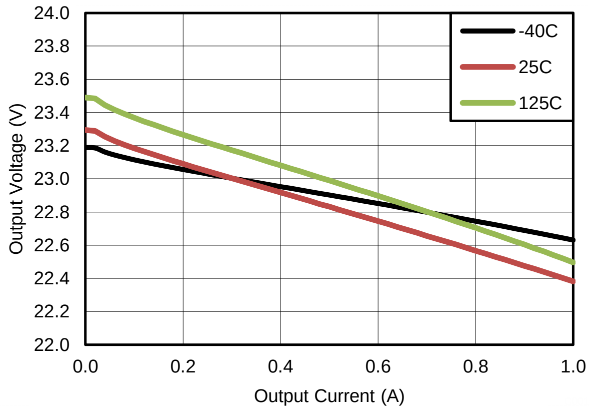


Figure 1. V_{OH} vs I_{OH}

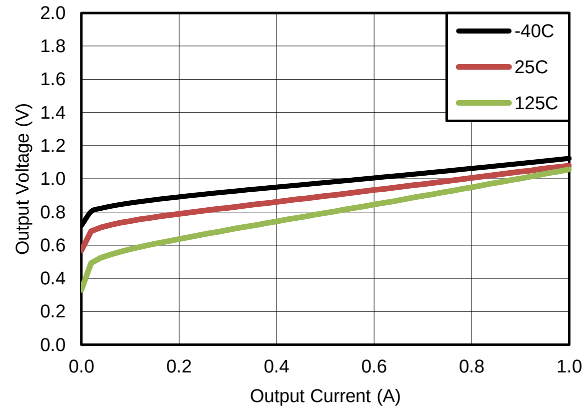
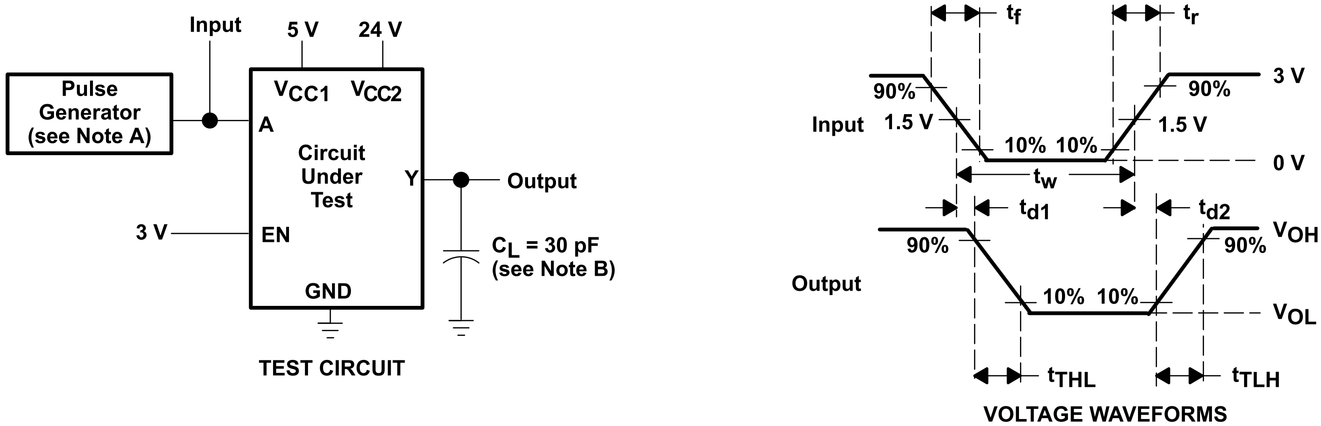


Figure 2. V_{OL} vs I_{OL}

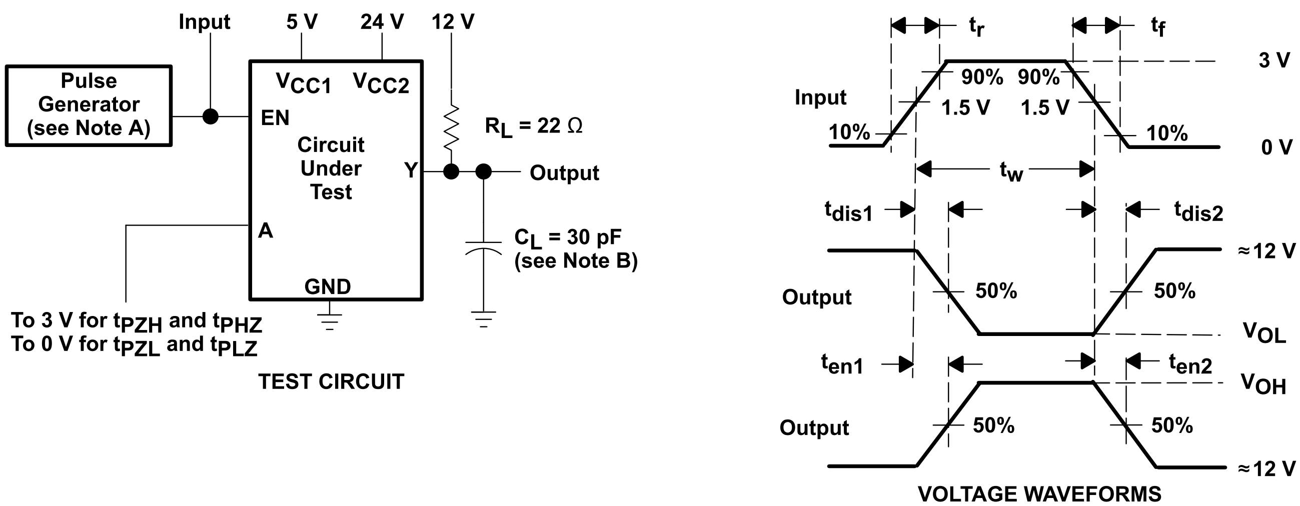
8 Parameter Measurement Information



A. The pulse generator has the following characteristics: t_r ≤10 ns, t_f ≤10 ns, t_w = 10 µs, P_{RR} = 5 kHz, Z_O = 50 Ω

B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Switching Times from Data Inputs



A. The pulse generator has the following characteristics: t_r ≤10 ns, t_f ≤10 ns, t_w = 10 µs, P_{RR} = 5 kHz, Z_O = 50 Ω

B. C_L includes probe and jig capacitance.

Figure 4. Test Circuit and Switching Times from Enable Inputs

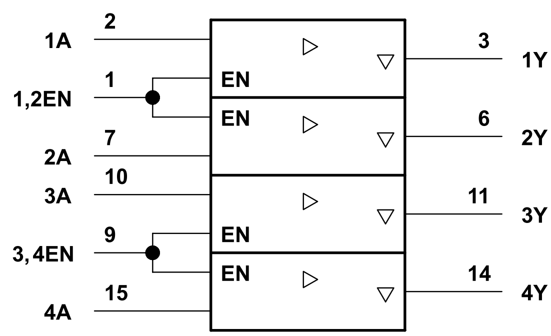
9 Detailed Description

9.1 Overview

The SN754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents up to 1 A at voltages from 4.5 V to 36 V. The device is designed to drive inductive loads such as relays, solenoids, DC and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications. All inputs are compatible with TTL and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage V_{CC2} is used for the output circuits. The SN754410 is designed for operation from −40°C to 85°C.

9.2 Functional Block Diagram



This symbol is in accordance with ANSI/IEEE Std 91-1984and IEC Publication 617-12.

9.3 Feature Description

9.3.1 High Current, High Voltage Outputs

Four high current and high voltage outputs feature clamp diodes for inductive load driving.

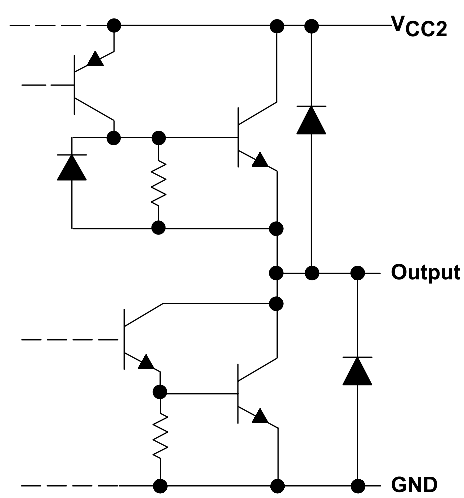


Figure 5. Typical of All Outputs

Feature Description (continued)

9.3.2 TTL Compatible Inputs

Data inputs and enable inputs are compatible with TTL. 3.3-V CMOS logic is also acceptable, however open or high impedance input voltage can approach V_{CC1} voltage.

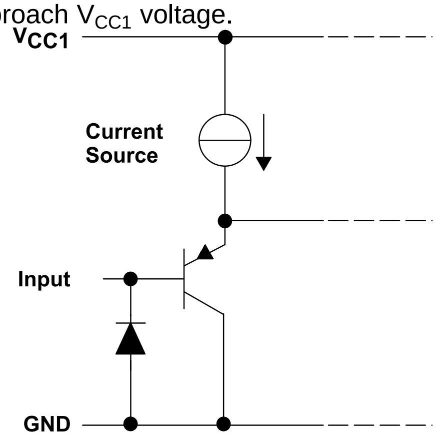


Figure 6. Equivalent of Each Input

9.4 Device Functional Modes

Table 1. Function Table(1)

INPUTS(2)		OUTPUTS
A	EN	Y
H	H	H
L	H	L
X	L	Z

(1) H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

(2) In the thermal shutdown mode, the output is in a high-impedance state regardless of the input levels.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Provide a 5-V supply to V_{CC1} and valid logic input levels to data and enable inputs. V_{CC2} must be connected to a power supply capable of suppling the needed current and voltage demand for the loads connected to the outputs.

10.2 Typical Application

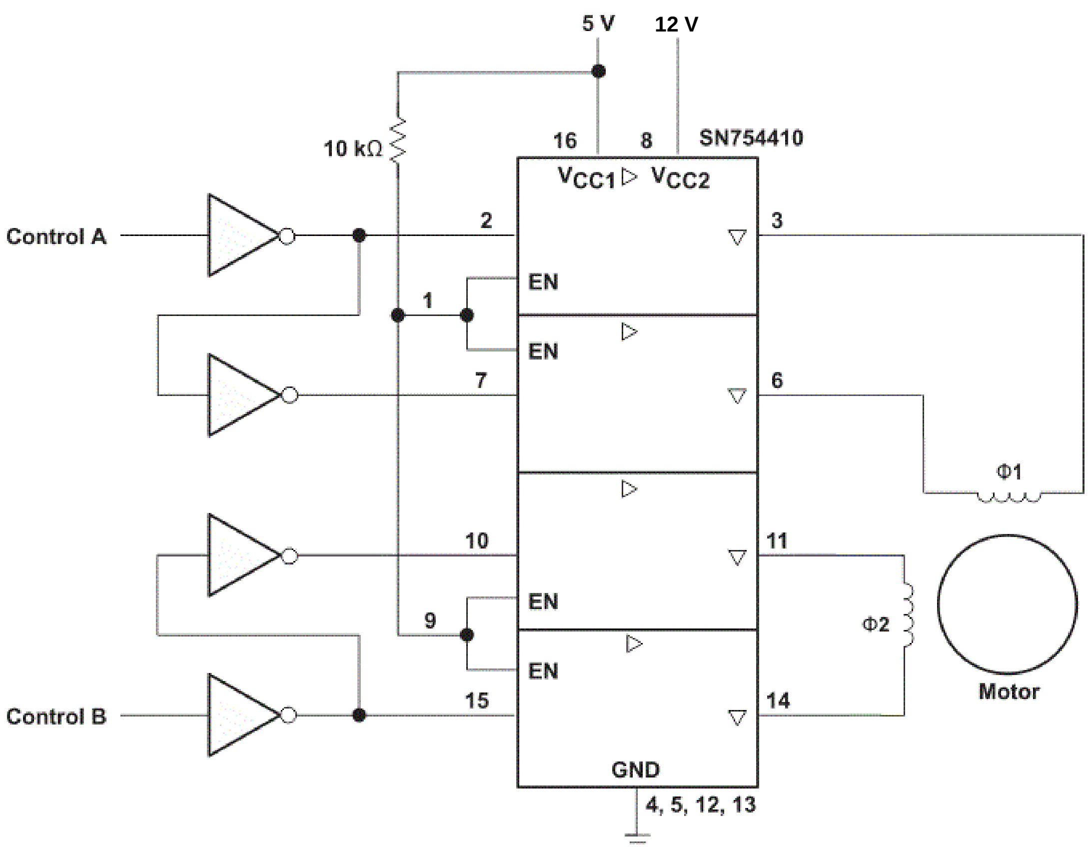


Figure 7. Typical Application Schematic

10.2.1 Design Requirements

The design techniques in the following sections may be used for applications which fall within the following requirements.

- 4.5-V minimum and 36-V maximum V_{CC2} voltage
- 1000-mA or less output current per channel
- 5-V supply with 10% tolerance or less
- TTL compatible logic inputs

Typical Application (continued)

10.2.2 Application Curves

Driver output voltage waveform with a two phase stepper motor; 12-V 20-Ω coils.

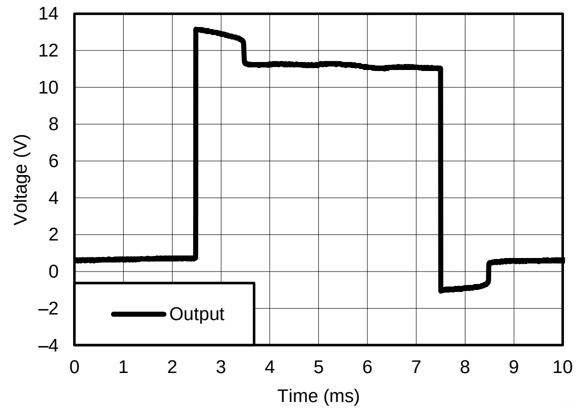


Figure 8. 100 Hz Driver Output Waveform

11 Power Supply Recommendations

V_{CC1} is 5 V ± 0.5 V and V_{CC2} can be same supply as V_{CC1} or a higher voltage supply with peak voltage up to 36 V. Bypass capacitors of 0.1 uF or greater should be used at V_{CC1} and V_{CC2} pins. There are no power up or power down supply sequence order requirements.

12 Layout

12.1 Layout Guidelines

Place device near the load to keep output traces short to reduce EMI. Use solid vias to transfer heat from ground pins to circuit board's ground plane.

12.2 Layout Example

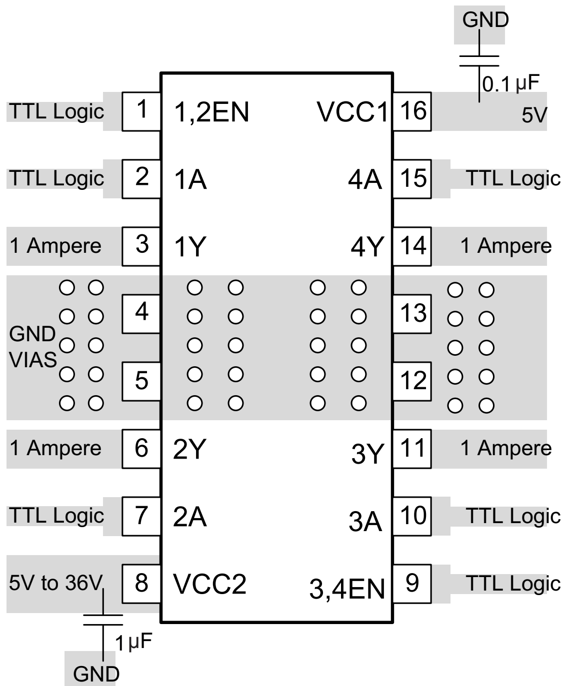


Figure 9. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)
SN754410NE	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN754410NE
SN754410NEE4	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN754410NE

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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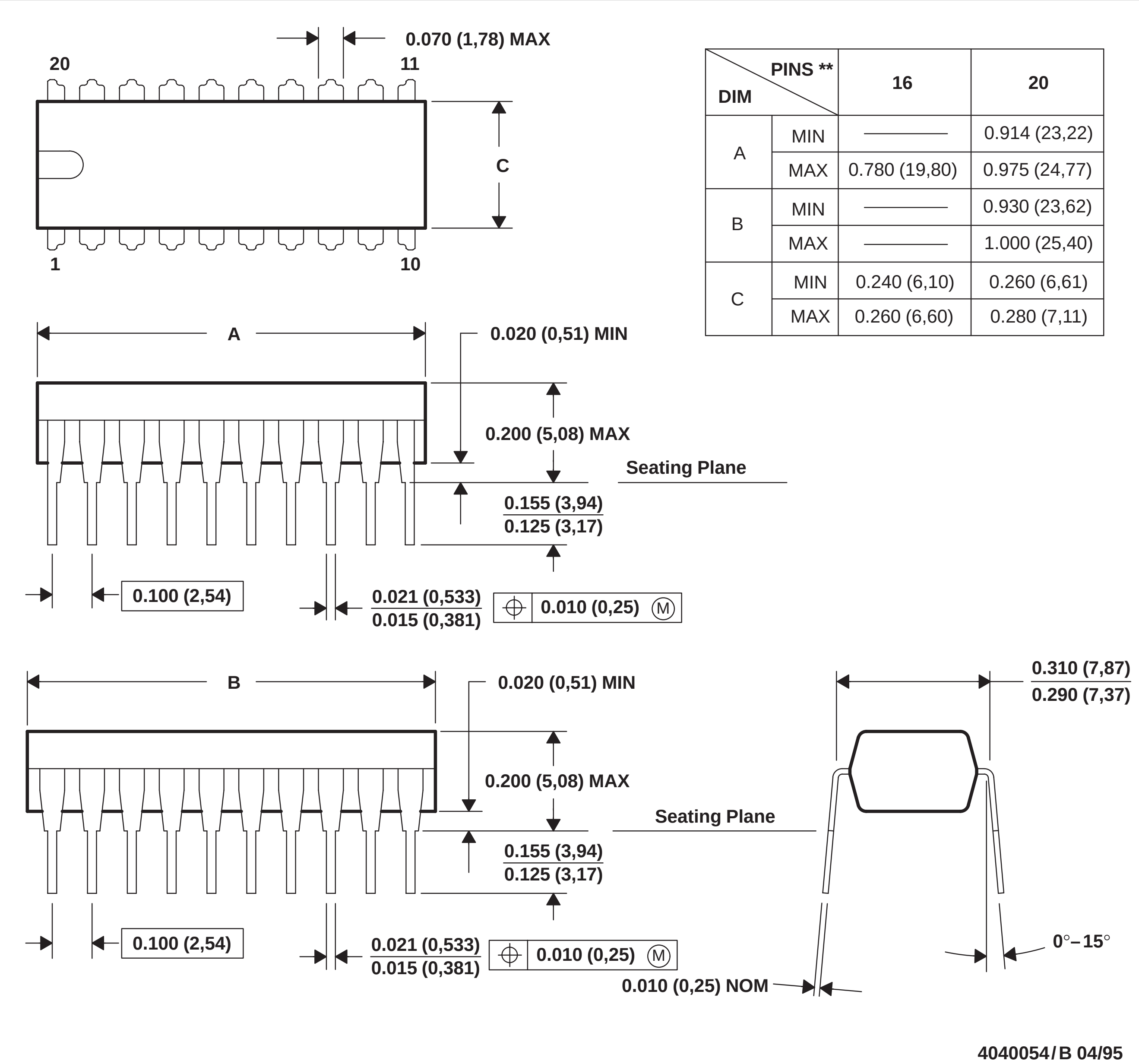
NE (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

20 PIN SHOWN



DIM	PINS **	16	20
A	MIN	———	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	———	0.930 (23,62)
	MAX	———	1.000 (25,40)
C	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 (16 pin only)

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