TLC555 CMOS Timer

1 Features

- Very low power consumption:
  - 1mW typical at V_{DD} = 5V
- Capable of operation in astable mode
- CMOS output capable of swinging rail to rail
- High output current capability
  - Sink: 100mA typical
  - Source: 10mA typical
- Output fully compatible with CMOS, TTL, and MOS
- Low supply current reduces spikes during output transitions
- Single-supply operation from 2V to 15V
- Functionally interchangeable with the NE555; has same pinout
- ESD protection exceeds 1000V per ANSI/ESDA/JEDEC JS-001
- Available in Q-temp automotive
  - High-reliability automotive applications
  - Configuration control and print support
  - Qualification to automotive standards

2 Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

3 Description

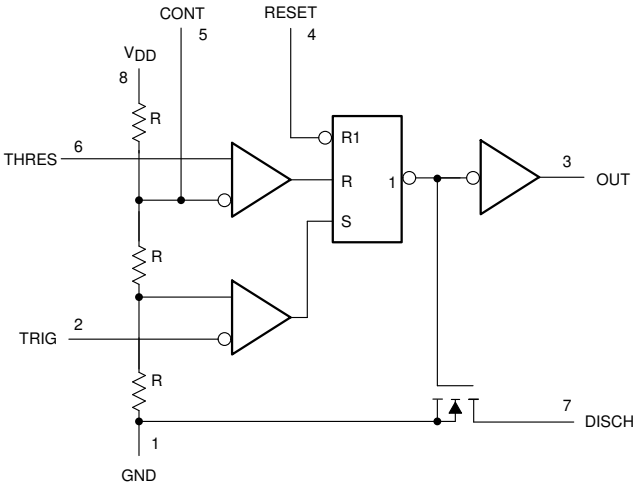
The TLC555 is a CMOS monolithic timing circuit. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2MHz. Because of a high input impedance, this device supports smaller timing capacitors than those supported by the NE555 or LM555. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power-supply voltage.

Like the NE555, the TLC555 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal (CONT). When the trigger input (TRIG) falls below the trigger level, the flip-flop is set and the output goes high. If TRIG is above the trigger level and the threshold input (THRES) is above the threshold level, the flip-flop is reset and the output is low. The reset input (RESET) can override all other inputs and can be used to initiate a new timing cycle. If RESET is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal (DISCH) and GND. All unused inputs must be tied to an appropriate logic level to prevent false triggering.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLC555C	SOIC (8)	4.9mm × 6.0mm
	PDIP (8)	9.81mm × 9.43mm
	SOP (8)	6.2mm × 7.8mm
	TSSOP (14)	5.0mm × 6.4mm
TLC555I	SOIC (8)	4.9mm × 6.0mm
	PDIP (8)	9.81mm × 9.43mm
TLC555M	LCCC (20)	8.89mm × 8.89mm
	CDIP (8)	9.6mm × 9.0mm
TLC555Q	SOIC (8)	4.9mm × 6.0mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

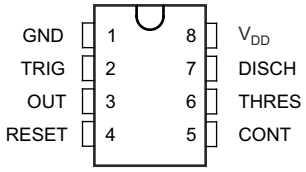

Figure 4-1. D, P, PS, and JG Packages, 8-Pin SOIC, PDIP, SOP, and CDIP (Top View)

Table 4-1. Pin Functions: D, P, PS, and JG Packages

PIN		TYPE	DESCRIPTION
NAME	NO.		
CONT	5	Input	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
DISCH	7	Output	Open collector output to discharge timing capacitor.
GND	1	—	Ground.
NC	—	—	No internal connection.
OUT	3	Output	High current timer output signal.
RESET	4	Input	Active low reset input forces output and discharge low.
THRES	6	Input	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	2	Input	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V_{DD}	8	—	Power-supply voltage.

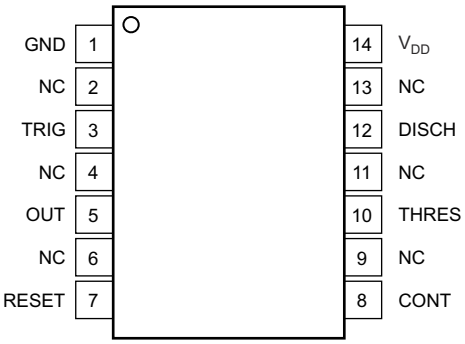

Figure 4-2. PW Package, 14-Pin TSSOP (Top View)

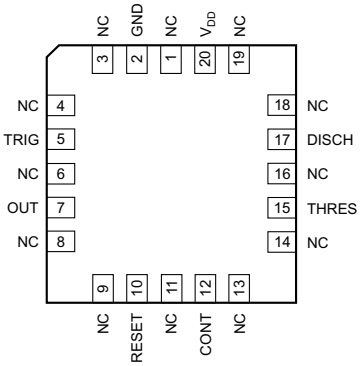

Figure 4-3. FK Package, 20-Pin LCCC (Top View)

Table 4-2. Pin Functions: PW and FK

PIN			TYPE	DESCRIPTION
NAME	NO.			
	PW (TSSOP)	FK (LCCC)		
CONT	8	12	Input	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
DISCH	12	17	Output	Open-collector output to discharge timing capacitor.
GND	1	2	—	Ground.
NC	2, 4, 6, 9, 11, 13	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	No internal connection.
OUT	5	7	Output	High current timer output signal.
RESET	7	10	Input	Active low reset input forces output and discharge low.
THRES	10	15	Input	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	3	5	Input	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V_{DD}	14	20	—	Power-supply voltage.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Voltage	Supply, V_{DD} (2)	–0.3	18	V
		Input, any input	–0.3	V_{DD}	
		Discharge	–0.3	18	
	Current	Sink, discharge or output		150	mA
		Source, output, I_O		15	
T_A	Operating temperature	C-suffix	0	70	°C
		I-suffix	–40	85	
		Q-suffix	–40	125	
		M-suffix	–55	125	
	Case temperature, for 60 seconds	FK package	–65	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(3)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) See Section 7.2.5 for application guidance on protecting the device against ESD.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	TLC555C	2	15	V
		TLC555I	3	15	
		TLC555M	5	15	
		TLC555Q	5	15	
T_A	Operating free-air temperature	TLC555C	0	70	°C
		TLC555I	–40	85	
		TLC555M	–55	125	
		TLC555Q	–40	125	

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5.4 Thermal Information

THERMAL METRIC[1]		TLC555						UNIT
		D (SOIC)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SOP)	PW (TSSOP)	
		8 PINS	20 PINS	8 PINS	8 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.9	N/A	120	93.1	120	135	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	37	81	82.5	72	61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.9	36	110	69.6	69	77	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.2	N/A	45	52.0	32	12	°C/W
ψ_{JB}	Junction-to-board characterization parameter	86.9	N/A	103	69.2	68	77	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.3	31	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics: V_{DD} = 2V for TLC555C, V_{DD} = 3V for TLC555I

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C	TLC555C	0.95	1.33	1.65	V
			TLC555I	1.6		2.4	
		Full range	TLC555C	0.85		1.75	
			TLC555I	1.5		2.5	
I_{IT}	Threshold current	25°C	TLC555C		10		pA
			TLC555I		10		
		Max	TLC555C		75		
			TLC555I		150		
$V_{I(TRIG)}$	Trigger voltage	25°C	TLC555C	0.4	0.67	0.95	V
			TLC555I	0.71	1	1.29	
		Full range	TLC555C	0.3		1.05	
			TLC555I	0.61		1.39	
$I_{I(TRIG)}$	Trigger current	25°C	TLC555C		10		pA
			TLC555I		10		
		Max	TLC555C		75		
			TLC555I		150		
$V_{I(RESET)}$	Reset voltage	25°C	TLC555C	0.4	1.1	1.5	V
			TLC555I	0.4	1.1	1.5	
		Full range	TLC555C	0.3		2	
			TLC555I	0.3		1.8	
	Control voltage (open-circuit) as a percentage of supply voltage	Max	TLC555C		66.7%		
			TLC555I		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 1mA, 25°C	TLC555C		0.03	0.2	V
			TLC555I		0.03	0.2	
		I_{OL} = 1mA, Full range	TLC555C			0.25	
			TLC555I			0.375	
	Discharge switch off-stage current	25°C	TLC555C		0.33		nA
			TLC555I		0.33		
		Max	TLC555C		11		
			TLC555I		30		
V_{OH}	High-level output voltage	I_{OH} = –300µA, 25°C	TLC555C	1.5	1.9		V
			TLC555I	2.5	2.85		
		I_{OH} = –300µA, Full range	TLC555C	1.5			
			TLC555I	2.5			
V_{OL}	Low-level output voltage	I_{OL} = 1mA, 25°C	TLC555C		0.07	0.3	V
			TLC555I		0.07	0.3	
		I_{OL} = 1mA, Full range	TLC555C			0.35	
			TLC555I			0.4	
I_{DD}	Supply current[2]	25°C	TLC555C			250	µA
			TLC555I			250	
		Full range	TLC555C			400	
			TLC555I			500	
C_{PD}	Power dissipation capacitance[3] [4]	25°C	TLC555C		80		pF
			TLC555I		90		

(1) Full range is 0°C to 70°C the for TLC555C, and –40°C to +85°C for the TLC555I. For conditions shown as MAX, use the appropriate value specified in the *Section 5.3*.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.
(3) C_{PD} is used to determine the dynamic power consumption.

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(4) $P_D = V_{DD}{}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage.

5.6 Electrical Characteristics: V_{DD} = 5V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	2.8	3.3	3.8	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	2.7		3.9	
I_{IT}	Threshold current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
$V_{I(TRIG)}$	Trigger voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	1.36	1.66	1.96	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	1.26		2.06	
$I_{I(TRIG)}$	Trigger current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
C_I	Trigger, threshold capacitance (each pin)	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		2.1		pF
$V_{I(RESET)}$	Reset voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	0.4	1.1	1.5	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	0.3		1.8	
$I_{I(RESET)}$	Reset current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
	Control voltage (open circuit) as a percentage of supply voltage	Max	TLC555C, TLC555I, TLC555M, TLC555Q		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 10mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.06	0.5	V
		I_{OL} = 10mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q			0.6	
	Discharge switch off-stage current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.3		nA
		Max	TLC555C		11		
			TLC555I		30		
			TLC555M, TLC555Q		275		
V_{OH}	High-level output voltage	I_{OH} = –1 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q	4.1	4.8		V
		I_{OH} = –1 mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q	4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.21	0.4	V
		I_{OL} = 8mA, Full range	TLC555C			0.5	
			TLC555I			0.5	
			TLC555M, TLC555Q			0.6	

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5.6 Electrical Characteristics: V_{DD} = 5V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 5mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.13	0.3	V
		I_{OL} = 5mA, Full range	TLC555C			0.4	
			TLC555I			0.4	
			TLC555M, TLC555Q			0.45	
		I_{OL} = 3.2mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.08	0.3	
		I_{OL} = 3.2mA, Full range	TLC555C			0.35	
			TLC555I			0.35	
			TLC555M, TLC555Q			0.4	
I_{DD}	Supply current[2]	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		180	350	µA
		Full range	TLC555C			500	
			TLC555I			600	
			TLC555M, TLC555Q			700	
C_{PD}	Power dissipation capacitance[3] [4]	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		115		pF

(1) Full range is 0°C to 70°C the for TLC555C, –40°C to 85°C for the TLC555I, –40°C to 125°C for the TLC555Q, and –55°C to 125°C for the TLC555M. For conditions shown as MAX, use the appropriate value specified in the *Section 5.3* table.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.
(3) C_{PD} is used to determine the dynamic power consumption.
(4) $P_D = V_{DD}{}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage.

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5.7 Electrical Characteristics: V_{DD} = 15V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	9.45	10	10.55	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	9.35		10.65	
I_{IT}	Threshold current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
$V_{I(TRIG)}$	Trigger voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	4.65	5	5.35	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	4.55		5.45	
$I_{I(TRIG)}$	Trigger current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
C_I	Trigger, threshold capacitance (each pin)	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		1.8		pF
$V_{I(RESET)}$	Reset voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	0.4	1.1	1.5	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	0.3		1.8	
$I_{I(RESET)}$	Reset current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
	Control voltage (open circuit) as a percentage of supply voltage	Max	TLC555C, TLC555I, TLC555M, TLC555Q		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 100mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.77	1.7	V
		I_{OL} = 100mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q			1.8	
	Discharge switch off-stage current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.75		nA
		Max	TLC555C		13		
			TLC555I		30		
			TLC555M, TLC555Q		280		
V_{OH}	High-level output voltage	I_{OH} = –10mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q	12.5	14.2		V
		I_{OH} = –10mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q	12.5			
		I_{OH} = –5mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q	13.5	14.6		
		I_{OH} = –5mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q	13.5			
		I_{OH} = –1mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q	14.2	14.9		
		I_{OH} = –1mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q	14.2			

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5.7 Electrical Characteristics: V_{DD} = 15V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 100mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		1.28	3.2	V
		I_{OL} = 100mA, Full range	TLC555C			3.6	
			TLC555I			3.7	
			TLC555M, TLC555Q			3.8	
		I_{OL} = 50mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.63	1	
		I_{OL} = 50mA, Full range	TLC555C			1.3	
			TLC555I			1.4	
			TLC555M, TLC555Q			1.5	
		I_{OL} = 10mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.12	0.3	
		I_{OL} = 10mA, Full range	TLC555C			0.4	
			TLC555I			0.4	
			TLC555M, TLC555Q			0.45	
I_{DD}	Supply current[2]	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		235	600	µA
		Full range	TLC555C			800	
			TLC555I			900	
			TLC555M, TLC555Q			1000	
C_{PD}	Power dissipation capacitance[3] [4]	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		140		pF

(1) Full range is 0°C to 70°C for TLC555C, –40°C to 85°C for TLC555I, –40°C to 125°C for the TLC555Q, and –55°C to 125°C for TLC555M. For conditions shown as MAX, use the appropriate value specified in the *Section 5.3* table.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.
(3) C_{PD} is used to determine the dynamic power consumption.
(4) $P_D = V_{DD}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage.

5.8 Timing Characteristics

V_{DD} = 5V, T_A = 25°C (unless otherwise noted). Characteristic values are specified by design, characterization, or both.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Supply voltage sensitivity of timing interval	V_{DD} = 5V to 15V, C_T = 0.1µF $R_A = R_B$ = 1kΩ to 100kΩ [1]		0.1	0.5	%/V
t_r	Output pulse rise time	R_L = 10MΩ, C_L = 10pF		20	75	ns
t_f	Output pulse fall time	R_L = 10MΩ, C_L = 10pF		15	60	ns
f_{max}	Maximum frequency in a-stable mode	R_A = 470Ω, C_T = 200pF R_B = 200Ω [1]	1.2	2.1		MHz

(1) R_A, R_B, and C_T are as defined in Figure 6-5.

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5.9 Typical Characteristics

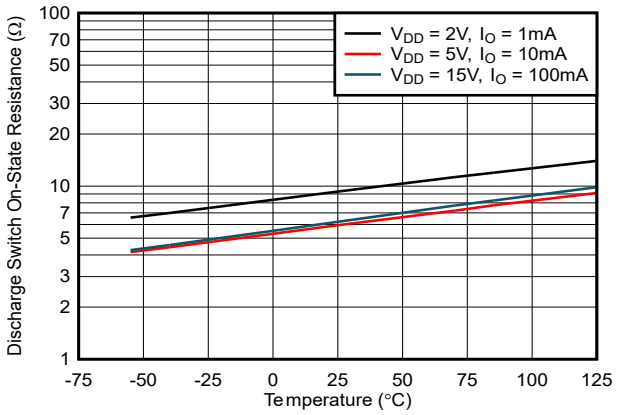

Figure 5-1. Discharge Switch On-State Resistance vs Free-Air Temperature

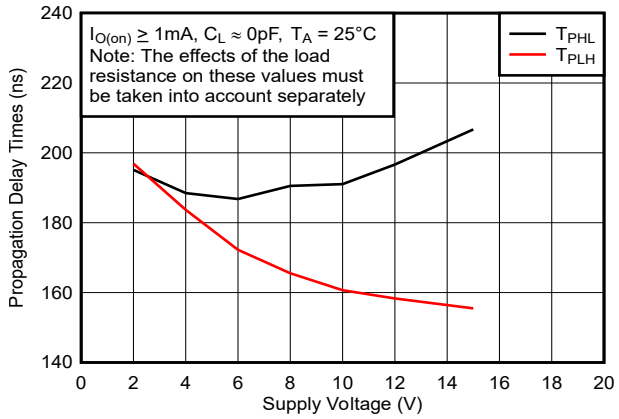

Figure 5-2. Propagation Delay Times to Discharge Output From Trigger and Threshold Shorted Together vs Supply Voltage

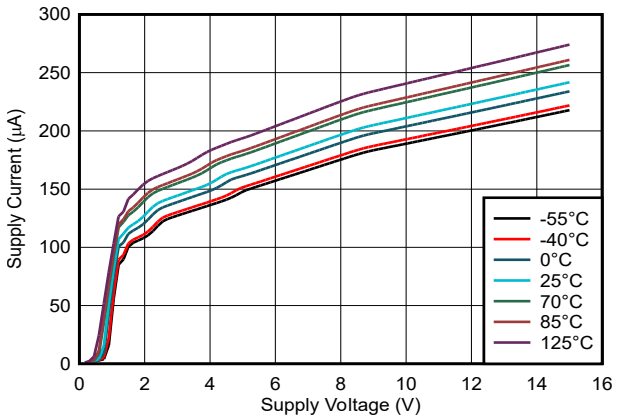

Figure 5-3. Supply Current vs Supply Voltage

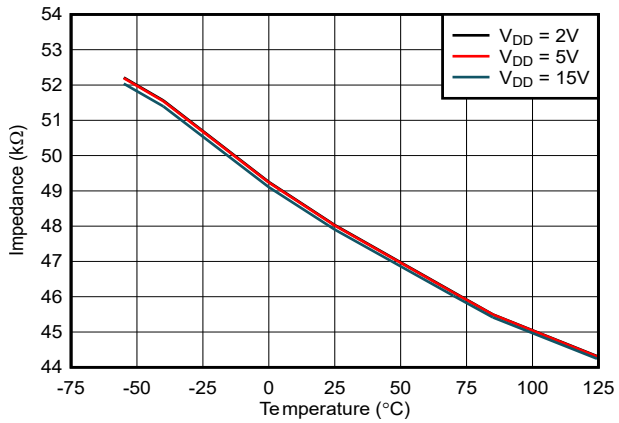

Figure 5-4. Control Impedance vs Temperature

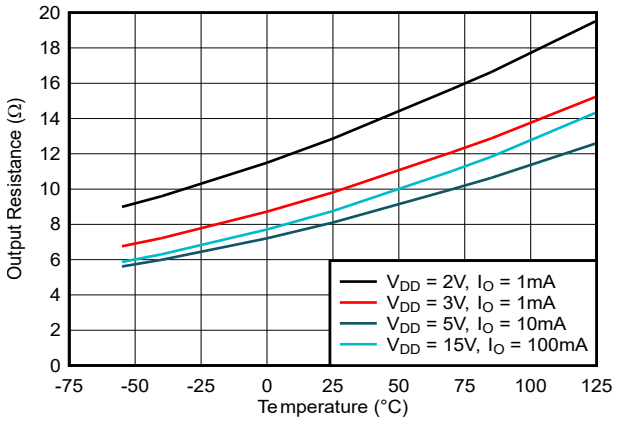

Figure 5-5. Output Low Resistance vs Temperature

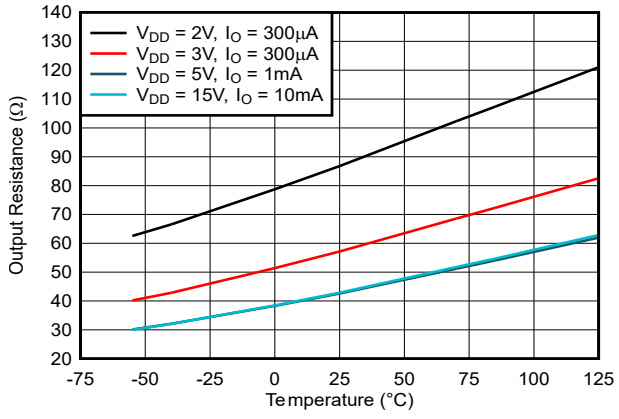

Figure 5-6. Output High Resistance vs Temperature

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5.9 Typical Characteristics (continued)

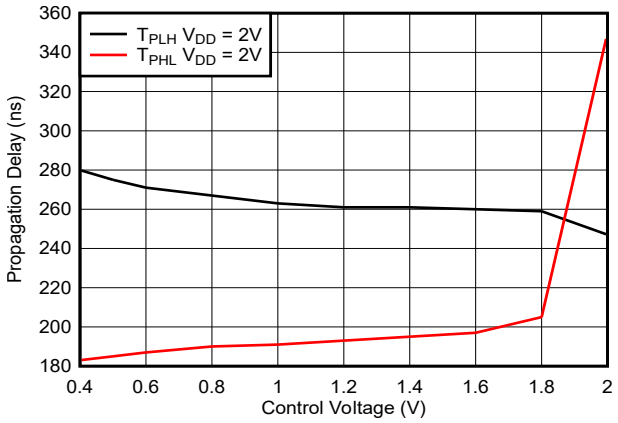

Figure 5-7. Propagation Delay vs Control Voltage

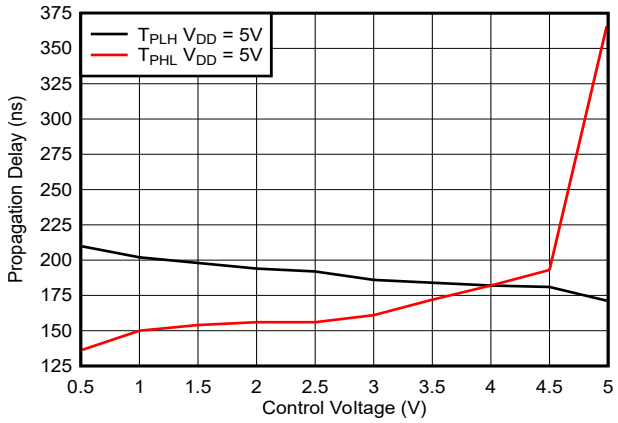

Figure 5-8. Propagation Delay vs Control Voltage

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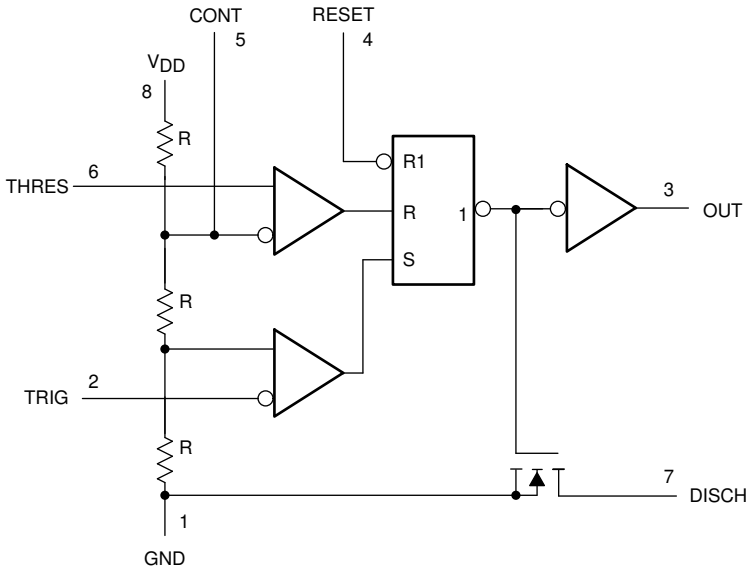
6 Detailed Description

6.1 Overview

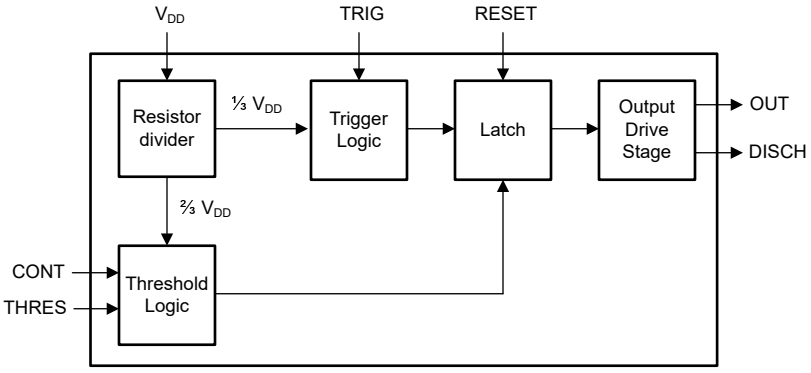
The TLC555 is a precision timing device used for general-purpose timing applications up to 2.1MHz. All inputs are level sensitive, not edge-triggered inputs.



Pin numbers are for all packages except PW and FK. RESET overrides TRIG, which overrides THRES (when CONT pin is 2/3 V_{DD}). The resistance of R resistors vary with V_{DD} and temperature. The resistors match each other very well across V_{DD} and temperature for a temperature-stable control-voltage ratio.

Figure 6-1. Simplified Schematic

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Monostable Operation

For monostable operation, Figure 6-2 shows how any of these timers can be connected. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the internal latch; the output goes high, and discharge pin (DISCH) becomes open drain. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the internal latch, the output goes low, the discharge pin goes low, which quickly discharges capacitor C.

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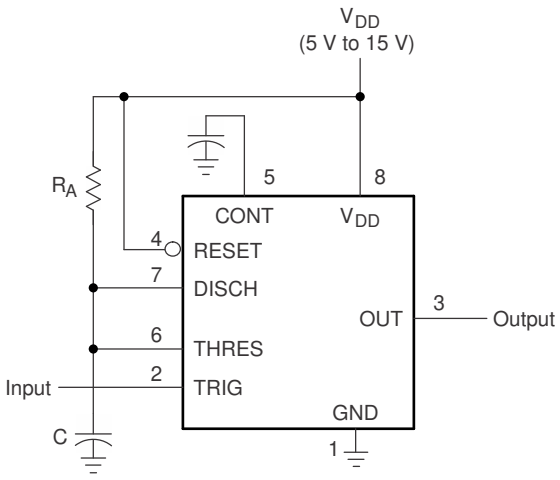

Figure 6-2. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage is less than the trigger threshold. If initiated, the sequence ends only if TRIG is high for at least 1µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 1µs, which limits the minimum monostable pulse duration to 1µs. The output pulse duration is approximately $t_w = 1.1 \times R_A C$. Figure 6-4 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{DD}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges capacitor C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not asserted low, RESET must be connected to V_{DD}. If the RESET function is required and the pin is driven by external logic or a microcontroller, use a pullup resistor to V_{DD} (such as 10 kΩ) to prevent the RESET pin from floating. If the RESET function is not required, short the RESET pin directly to the V_{DD} pin.

In monostable applications, set the trip point of the trigger input by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage, from a resistor divider with at least 500µA bias, provides good results.

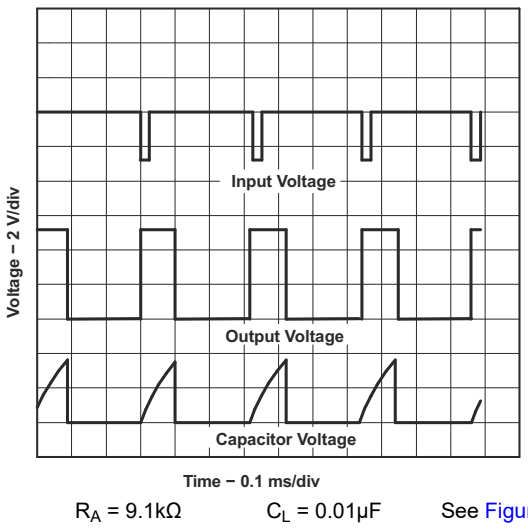

Figure 6-3. Typical Monostable Waveforms

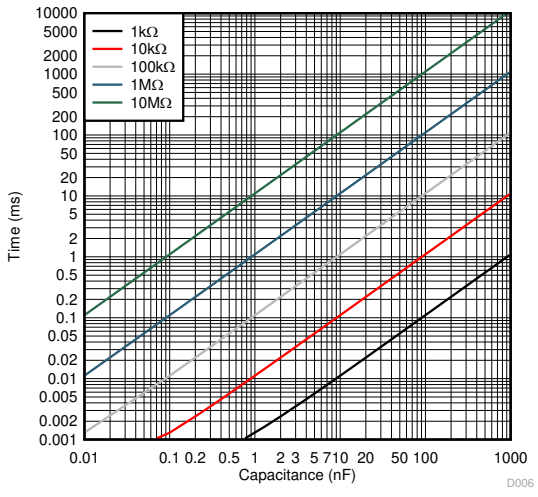

Figure 6-4. Output Pulse Duration vs Capacitance

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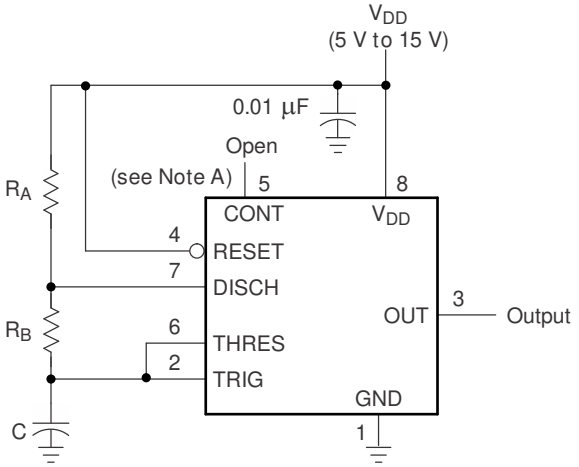
6.3.2 Astable Operation

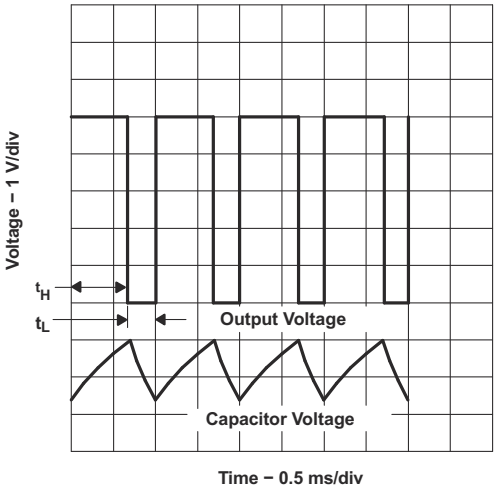
As shown in Figure 6-5, adding a second resistor, R_B, to the circuit of Figure 6-2 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (≈ 0.67 × V_{CC}) and the trigger-voltage level (≈ 0.33 × V_{CC}). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Decouple CONT voltage to ground with a capacitor to improve operation. Reevaluate for individual applications.

Figure 6-5. Circuit for Astable Operation



R_A = 5kΩ R_B = 3kΩ C = 0.15µF
See Figure 6-5

Figure 6-6. Typical Astable Waveforms

Figure 6-6 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L for frequencies below 100 kHz can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

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Equation 1 to Equation 7 do not account for any propagation delay times from the TRIG and THRES inputs to DISCH output. These delay times add directly to the period and overcharge the capacitor, which creates differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance r_{on} during discharge adds to R_B to provide another source of timing error in the calculation when R_B is very low. The following equations provide better agreement with measured values. The formulas in Equation 8 represent the actual low and high times when used at higher frequencies (beyond 100 kHz) because propagation delay and discharge on resistance is added to the formulas. The value of C_T includes both the nominal or deliberate timing capacitance, as well as parasitic capacitance on the PCB. Decoupling capacitance on CONT also affects the duty cycle, with an error contribution that depends on the capacitor leakage resistance. For additional discussion, see the *Design low-duty-cycle timer circuits* article.

$$t_{c(H)} = C_T\,(R_A + R_B)\,\ln\left[3 - \exp\left(\frac{-t_{PLH}}{C_T(R_B + r_{on})}\right)\right] + t_{PHL}$$

$$t_{c(L)} = C_T\,(R_B + r_{on})\,\ln\left[3 - \exp\left(\frac{-t_{PHL}}{C_T(R_A + R_B)}\right)\right] + t_{PLH} \quad (8)$$

These equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between ln(2) at low frequencies, and ln(3) at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Output waveform duty cycles less than 50% require that $t_{c(H)} / t_{c(L)} < 1$ and possibly that $R_A \leq r_{on}$. These conditions can be difficult to obtain. Figure 6-8 shows the nominal free-running frequency associated with various combinations of C_T and $R_A + 2 \times R_B$.

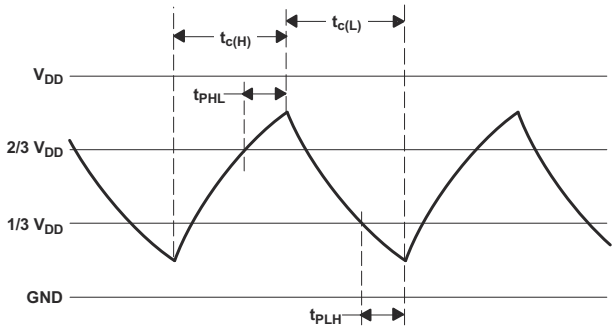

Figure 6-7. Trigger and Threshold Voltage Waveform

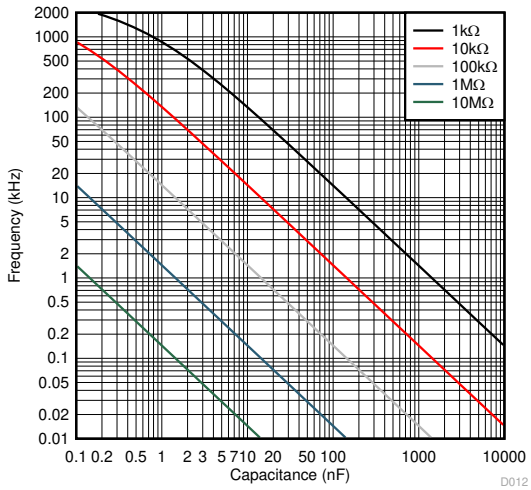

Figure 6-8. Nominal Free-Running Frequency vs Timing Capacitance
Resistance = R_A + 2 × R_B

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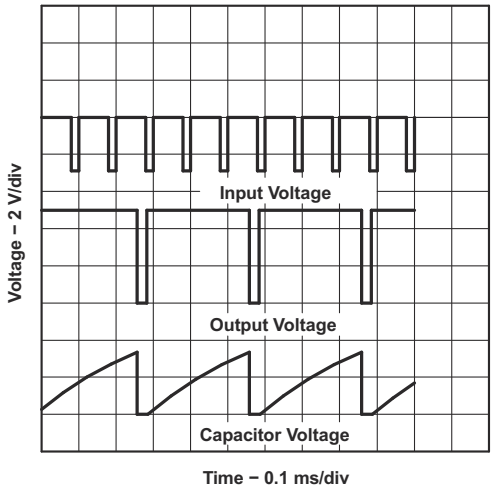
6.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 6-2 can be made to operate as a frequency divider. Figure 6-9 shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.



V_{CC} = 5V R_A = 1250Ω C = 0.2μF

See Figure 6-2

Figure 6-9. Divide-by-Three Circuit Waveforms

6.4 Device Functional Modes

Table 6-1 shows the device truth table. For a valid reset voltage condition, use an external pullup resistor to V_{DD} (if using the RESET functionality), or short the RESET pin directly to V_{DD} (if the RESET functionality is not used).

Table 6-1. Function Table

RESET VOLTAGE(1)	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
< MIN	Irrelevant	Irrelevant	L	On
> MAX	< MIN	Irrelevant(2)	H	Off
> MAX	> MAX	> MAX	L	On
> MAX	> MAX	< MIN	As previously established	

(1) For conditions shown as MIN or MAX, use the appropriate value specified under *Section 5.6*.
(2) CONT pin open or 2/3 V_{DD}.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLC555 timer device uses resistor and capacitor charging delay to provide a programmable time delay or operating frequency. *Section 7.2* presents a simplified discussion of the design process. Reset mode forces output and discharge low and provides a small reduction in supply current.

7.2 Typical Applications

7.2.1 Missing-Pulse Detector

The circuit shown in Figure 7-1 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 7-2.

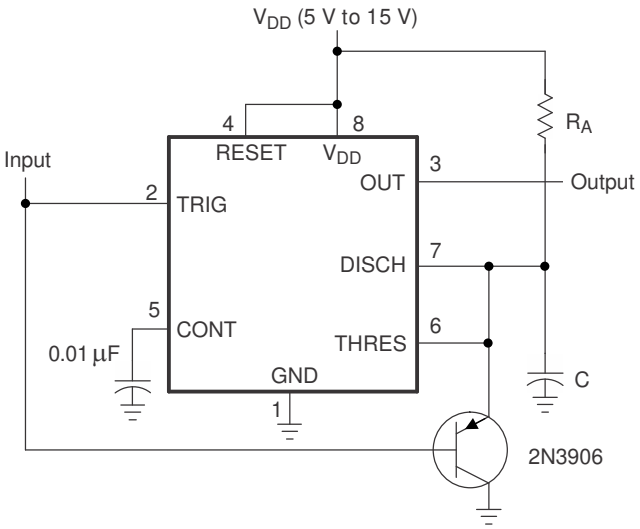

Figure 7-1. Circuit for Missing-Pulse Detector

7.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. An input stuck low cannot be detected because the timing capacitor (C) remains discharged.

7.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C >$ [maximum normal input high time].

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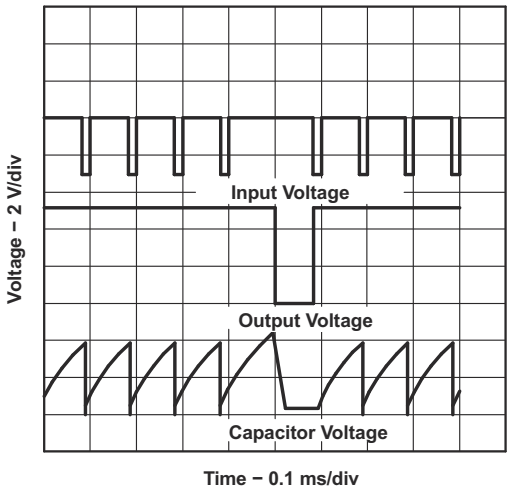
7.2.1.3 Application Curve



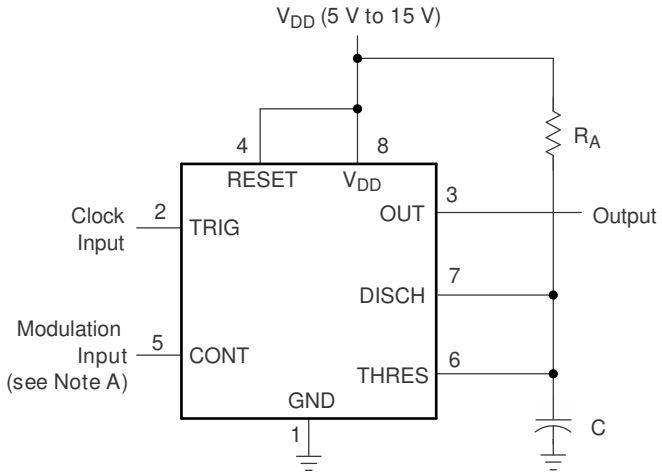
V_{DD} = 5V R_A = 1kΩ C = 0.1µF

See Figure 7-1

Figure 7-2. Timing Waveforms for Missing-Pulse Detector

7.2.2 Pulse-Width Modulation

To modify timer operation, apply an external voltage (or current) to CONT to modulate the internal threshold and trigger voltages. Figure 7-3 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 7-4 shows the resulting duty cycle versus control voltage transfer function. Attempting to run under 10% duty cycle can result in inconsistent output pulses. Attempting to run close to 100% duty cycle results in frequency division by 2, then 3, then 4.



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

Figure 7-3. Circuit for Pulse-Width Modulation

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7.2.2.1 Design Requirements

The clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 V_{DD}, respectively. Clock input V_{OL} time must be less than minimum output high time; therefore, a high (positive) duty cycle clock is recommended. Minimum recommended modulation voltage is 1V. Lower CONT voltage can greatly increase threshold comparator propagation delay and storage time. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is RC-based with an negative exponential curve.

7.2.2.2 Detailed Design Procedure

Choose R_A and C so that R_A × C is same or less than clock input period. Figure 7-4 shows the non linear relationship between control voltage and output duty cycle. Duty cycle is function of control voltage and clock period relative to RC time constant.

7.2.2.3 Application Curve

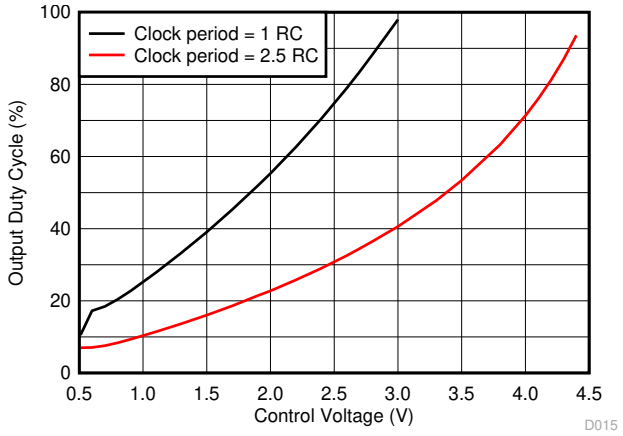
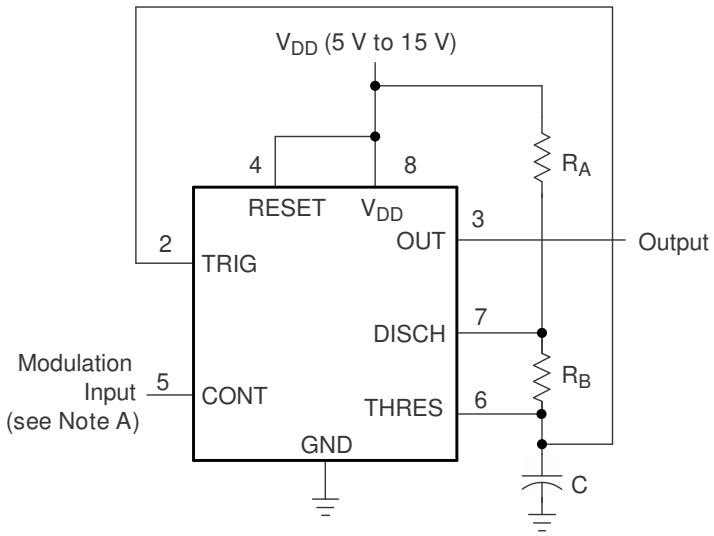


Figure 7-4. Pulse-Width-Modulation vs Control Voltage Clock Duty Cycle 98%, V_{DD} = 5V

7.2.3 Pulse-Position Modulation

As shown in Figure 7-5, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and thereby the time delay of a free-running oscillator. Figure 7-6 and Figure 7-7 shows the output frequency and duty cycle versus control voltage.



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

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R_A = 3kΩ R_B = 309kΩ C = 1nF

Figure 7-5. Circuit for Pulse-Position Modulation

7.2.3.1 Design Requirements

Both dc- and ac-coupled modulation input changes the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle vary with the modulation voltage. Control voltage less than 1V can result in output glitches instead of a steady-output pulse stream

7.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle for control voltage set to 2/3 of V_{DD} can be determined using formulas in *Section 6.3.2* section.

7.2.3.3 Application Curves

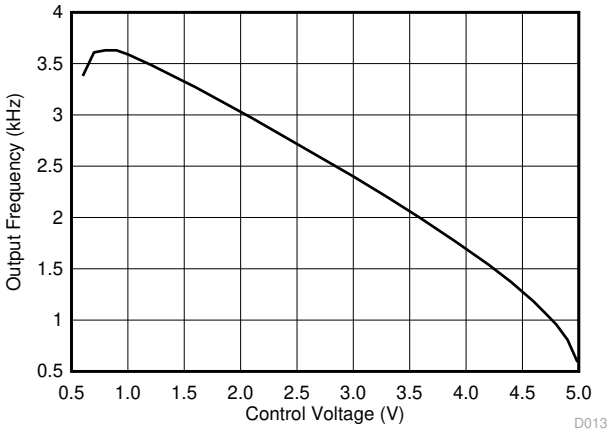

Figure 7-6. Pulse-Position-Modulation Frequency vs Control Voltage, V_{DD} = 5V

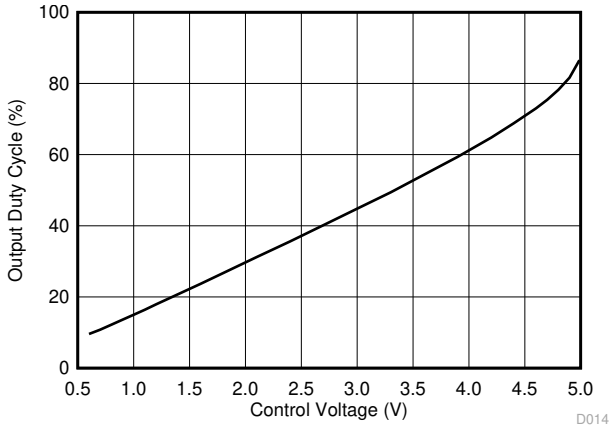

Figure 7-7. Pulse-Position-Modulation Duty Cycle vs Control Voltage, V_{DD} = 5V

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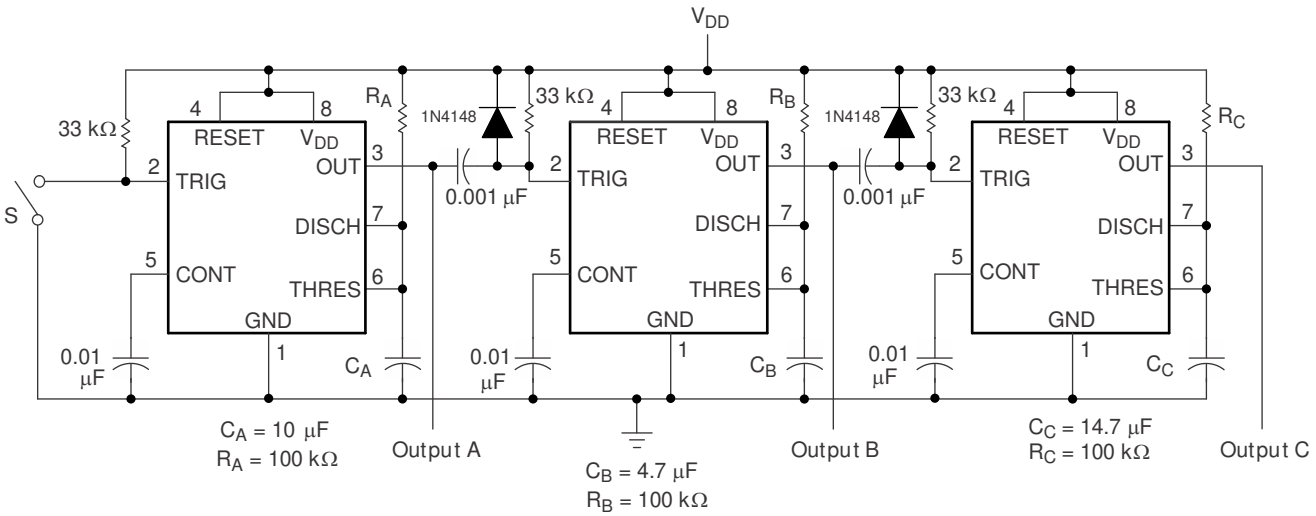
7.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 7-8 shows a sequencer circuit with possible applications in many systems, and Figure 7-9 shows the output waveforms.



S closes momentarily at t = 0.

Figure 7-8. Sequential Timer Circuit

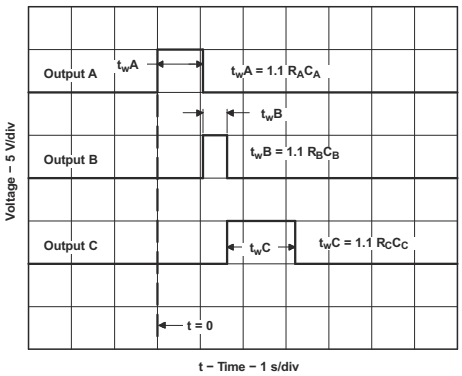
7.2.4.1 Design Requirements

The sequential-timer application chains together multiple monostable timers. The joining components are the 33kΩ resistors and 0.001µF capacitors. The output high-to-low edge passes a 10µs start pulse to the next monostable. A diode is required to prevent overvoltage on the trigger input when on the previous output low-to-high edge.

7.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula: $t_w = 1.1 \times R \times C$.

7.2.4.3 Application Curve



See Figure 7-8

Figure 7-9. Sequential Timer Waveforms

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7.2.5 Designing for Improved ESD Performance

The TLC555 internal HBM and CDM protection allows for safe assembly in ESD-controlled environments. In applications that expose the pins of the TLC555 to ESD, additional protection is highly recommended. The following test board schematic has bypass capacitors, current-limiting resistors, and voltage-clamping TVS diodes to provide additional protection for commonly exposed pins (Reset, Trig, and Output) against ESD.

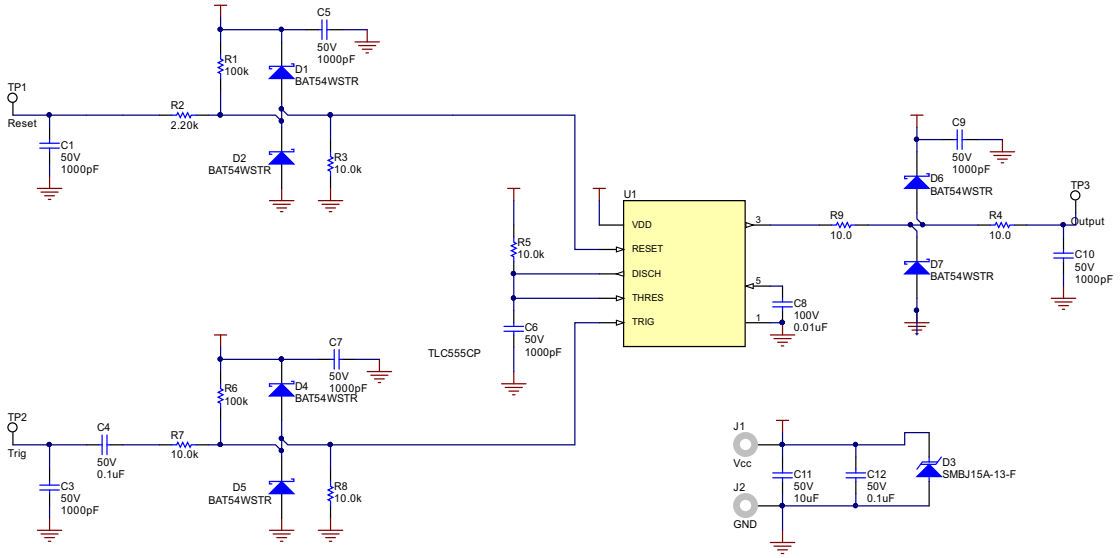

Figure 7-10. ESD Test Schematic

The following table gives the ESD protection levels recorded for different supply voltages and external components populated. Using only passive components to protect the TLC555 with a single 15V supply is not recommended because the higher voltage allows for an unacceptable amount of current to flow through the device.

Table 7-1. ESD Test Results

SUPPLY VOLTAGE	ONLY PASSIVE COMPONENTS POPULATED D1..D7 NOT POPULATED(1)	ALL COMPONENTS POPULATED (1)
5V	8kV	12kV
15V	Not recommended	12kV

(1) Sample results. Results can vary with populated components, board layout, and samples used.

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7.3 Power Supply Recommendations

The TLC555 requires a voltage supply greater than or equal to 2V, 3V, or 5V based the coldest ambient temperature supported and a supply voltage less than or equal to 15V. Adequate power supply bypassing is necessary to protect associated circuitry and provide stable output pulses. Minimum recommended is 0.1µF ceramic in parallel with 1µF electrolytic. Place the bypass capacitors as close as possible to the TLC555 and minimize the trace length.

7.4 Layout

7.4.1 Layout Guidelines

Standard PCB rules apply to routing the TLC555. The 0.1µF ceramic capacitor in parallel with a 1µF electrolytic capacitor must be as close as possible to the TLC555. The capacitor used for the time delay must also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

Figure 7-11 is the basic layout for various applications.

- C1—based on time delay calculations
- C2—0.01µF bypass capacitor for control voltage pin
- C3—0.1µF bypass ceramic capacitor
- C4—1µF electrolytic bypass capacitor
- R1—based on time-delay calculations

7.4.2 Layout Example

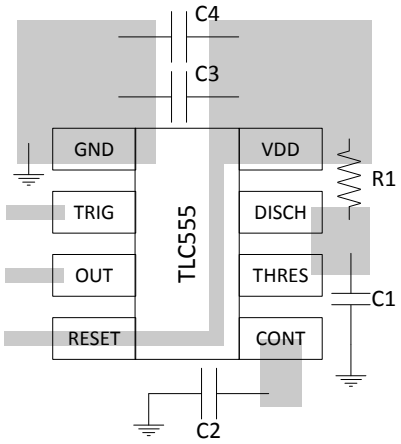

Figure 7-11. Layout Example

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8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (November 2023) to Revision K (January 2026) **Page**

- Removed LinCMOS™ terminology from data sheet....1
- Removed Machine Model (MM) specification from *ESD Ratings* table....4
- Changed the discharge switch off-stage current typical value for TLC555C at 25°C from 0.1nA to 0.33nA in *Electrical Characteristics: V_{DD} = 2V for TLC555C, V_{DD} = 3V for TLC555I* 6
- Changed the discharge switch off-stage current typical value for TLC555I at 25°C from 0.1nA to 0.33nA in *Electrical Characteristics: V_{DD} = 2V for TLC555C, V_{DD} = 3V for TLC555I* 6
- Changed the discharge switch off-stage current typical value for TLC555C across temperature from 0.5nA to 11nA in *Electrical Characteristics: V_{DD} = 2V for TLC555C, V_{DD} = 3V for TLC555I* 6
- Changed the discharge switch off-stage current typical value for TLC555I across temperature from 120nA to 30nA in *Electrical Characteristics: V_{DD} = 2V for TLC555C, V_{DD} = 3V for TLC555I* 6
- Removed reset current (I_{RESET}) typical specification with test condition V_{RESET} = 0V in *Electrical Characteristics: V_{DD} = 5V* 7
- Removed the test condition V_{RESET} = V_{DD} from reset current in *Electrical Characteristics: V_{DD} = 5V* 7
- Changed the typical value of discharge switch off-stage current at 25°C from 0.1nA to 0.3nA in *Electrical Characteristics: V_{DD} = 5V* 7
- Changed the typical value of discharge switch off-stage current for TLC555C at max temperature range from 0.5nA to 11nA in *Electrical Characteristics: V_{DD} = 5V* 7
- Changed the typical value of discharge switch off-stage current for TLC555I at max temperature range from 120nA to 30nA in *Electrical Characteristics: V_{DD} = 5V* 7
- Changed the typical value of discharge switch off-stage current for TLC555M and TLC555Q at max temperature range from 120nA to 275nA in *Electrical Characteristics: V_{DD} = 5V* 7
- Changed the typical value of discharge switch on-stage voltage at 25°C from 0.14V to 0.06V in *Electrical Characteristics: V_{DD} = 5V* 7
- Removed reset current (I_{RESET}) typical specification with test condition V_{RESET} = 0V in *Electrical Characteristics: V_{DD} = 15V* 9
- Removed the test condition V_{RESET} = V_{DD} from reset current in *Electrical Characteristics: V_{DD} = 15V* 9
- Changed the typical value of discharge switch off-stage current at 25°C from 0.1nA to 0.75nA in *Electrical Characteristics: V_{DD} = 15V* 9
- Changed the typical value of discharge switch off-stage current for TLC555C at max temperature range from 0.5nA to 13nA in *Electrical Characteristics: V_{DD} = 15V* 9
- Changed the typical value of discharge switch off-stage current for TLC555I at max temperature range from 120nA to 30nA in *Electrical Characteristics: V_{DD} = 15V* 9
- Changed the typical value of discharge switch off-stage current for TLC555M and TLC555Q at max temperature range from 120nA to 280nA in *Electrical Characteristics: V_{DD} = 15V* 9
- Changed the typical value of supply current at at 25°C from 360µA to 235µA in *Electrical Characteristics: V_{DD} = 15V* 9
- Updated all charts in the *Typical Characteristics* section....11

Changes from Revision I (July 2019) to Revision J (November 2023) **Page**

- Changed ESD protection specification from 2000V per MIL-STD-883C, method 3015.2, to 1000V per ANSI/ESDA/JEDEC JS-001, in *Features* 1
- Changed *Device Information* table to *Package Information*, and changed *Body Size (Nom)* to *Package Size*, in *Description* section....1
- Added *ESD Ratings* table and HBM, CDM, and MM specifications....4
- Changed thermal resistance and characterization parameter values for SOIC and PDIP packages in *Thermal Information* table....5

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- Changed reset current (I_{RESET}) test conditions to V_{RESET} = V_{DD}, in *Electrical Characteristics: V_{DD} = 5V* and *Electrical Characteristics: V_{DD} = 15V* 7
- Added new reset current (I_{RESET}) typical specification, for test condition V_{RESET} = 0V, to *Electrical Characteristics: V_{DD} = 5V* and *Electrical Characteristics: V_{DD} = 15V* 7
- Changed supply current (I_{DD}) typical value from 170µA to 180µA in *Electrical Characteristics: V_{DD} = 5V* 7
- Changed title of *Operating Characteristics* section to *Timing Characteristics* and clarified that values are specified by design or characterization..... 10
- Deleted Initial error of timing interval specification in *Timing Characteristics* 10
- Added Figure 5-4, *Supply Current vs Supply Voltage, Unit 2* 11
- Changed Figure 5-3, *Supply Current vs Supply Voltage*, to add "Unit 1" to title, and deleted 0°C and 70°C curves..... 11
- Changed functional block diagram to simplified schematic and moved to *Overview* 13
- Updated *Functional Block Diagram* 13
- Added guidance for RESET pin pullup resistance and CONT pin voltage range to *Monostable Operation* ... 13
- Added clarity regarding nominal operating frequency and parasitic terms in *Astable Operation* 15
- Deleted link to deprecated TLC555 Design Calculator in *Astable Operation* 15
- Deleted Figure 17, *Equivalent Schematic*, and added guidance concerning the RESET pin in *Device Functional Modes* 17

Changes from Revision H (August 2016) to Revision I (July 2019) **Page**

- Added MIN value for input voltage in *Absolute Maximum Ratings* 4
- Added discharge pin in *Absolute Maximum Ratings* 4
- Changed MIN supply voltage based on part number in *Recommended Operating Conditions* 4
- Added power dissipation capacitance TYP value in *Electrical Characteristics: V_{DD} = 2V for TLC555C, V_{DD} = 3V for TLC555I* 6
- Added trigger, threshold capacitance TYP value in *Electrical Characteristics: V_{DD} = 5V* 7
- Changed V_{OH} test condition current to –1mA in *Electrical Characteristics: V_{DD} = 5V* 7
- Added power dissipation capacitance TYP value in *Electrical Characteristics: V_{DD} = 5V* 7
- Added trigger, threshold capacitance TYP value in *Electrical Characteristics: V_{DD} = 15V* 9
- Added power dissipation capacitance TYP value in *Electrical Characteristics: V_{DD} = 15V* 9
- Added *Operating Characteristics* to the *Specifications* section..... 10
- Added Supply Current vs Supply Voltage chart to the *Typical Characteristics* section..... 11
- Added Control Impedance vs Temperature chart to the *Typical Characteristics* section..... 11
- Added Output Low Resistance vs Temperature chart to the *Typical Characteristics* section..... 11
- Added Output High Resistance vs Temperature chart to the *Typical Characteristics* section..... 11
- Added Propagation Delay vs Control Voltage chart, V_{DD} = 2V to the *Typical Characteristics* section..... 11
- Added Propagation Delay vs Control Voltage chart, V_{DD} = 5V to the *Typical Characteristics* section..... 11
- Changed trigger high hold time to 1µs in *Monostable Operation* 13
- Changed minimum monostable pulse width to 1µs in *Monostable Operation* 13
- Changed Output Pulse Duration vs Capacitance chart scale down to 0.001ms in *Monostable Operation* 13
- Added more astable frequency formulas to the *Astable Operation* section..... 15
- Changed scale on Free-Running Frequency vs Timing Capacitance chart up to 2MHz in the *Astable Operation* section..... 15
- Added CONT pin table note to the Table 6-1, *Function Table* in the *Device Functional Modes* 17
- Changed the application curve chart in the *Pulse-Width Modulation* section..... 20
- Changed the application curve charts in the *Pulse-Position Modulation* section..... 21
- Added clamping diodes to Sequential Timer Circuit in the *Sequential Timer* section..... 22
- Added *Designing for Improved ESD Performance* section to the *Application Information* section..... 23

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Changes from Revision G (November 2008) to Revision H (August 2016) **Page**

- Added *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.... 1
- Changed values in the *Thermal Information* table to align with JEDEC standards.... 5
- Deleted *Dissipation Ratings* table 5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-89503012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89503012A TLC555MFKB
5962-8950301PA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8950301PA TLC555M
TLC555CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	TL555C
TLC555CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL555C
TLC555CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL555C
TLC555CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC555CP
TLC555CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC555CP
TLC555CPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555
TLC555CPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555
TLC555CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555
TLC555CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555
TLC555CPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555
TLC555CPW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555
TLC555CPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555
TLC555CPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555
TLC555ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	TL555I
TLC555IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL555I
TLC555IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL555I
TLC555IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC555IP
TLC555IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC555IP
TLC555MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89503012A TLC555MFKB
TLC555MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89503012A TLC555MFKB
TLC555MJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC555MJG
TLC555MJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC555MJG

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC555MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8950301PA TLC555M
TLC555MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8950301PA TLC555M
TLC555QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL555Q
TLC555QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL555Q
TLC555QDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TL555Q
TLC555QDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL555Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLC555, TLC555M :

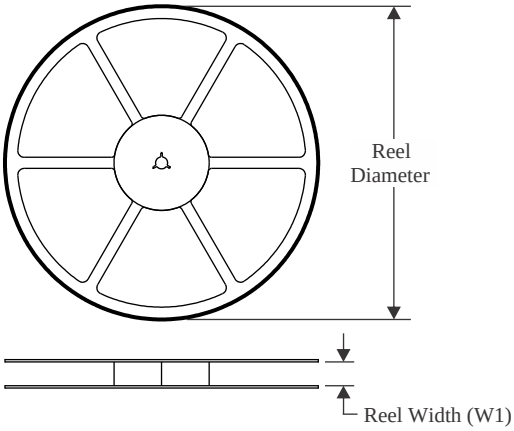
- Catalog : TLC555
- Automotive : TLC555-Q1, TLC555-Q1
- Military : TLC555M

NOTE: Qualified Version Definitions:

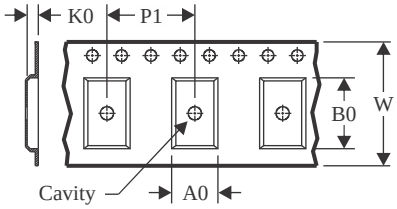
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

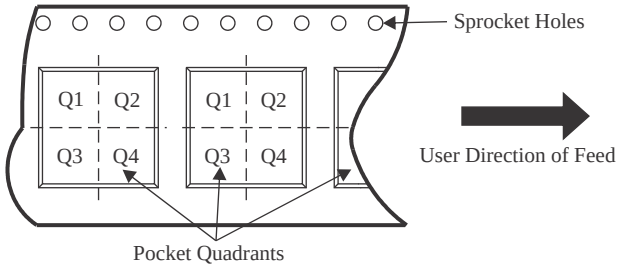


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

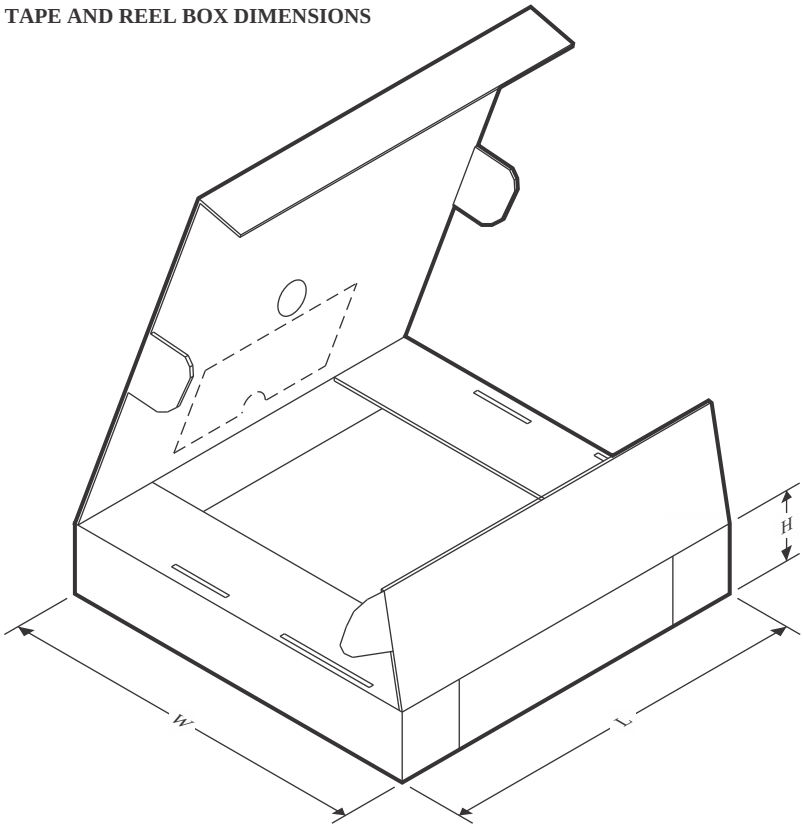
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC555CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC555CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC555IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

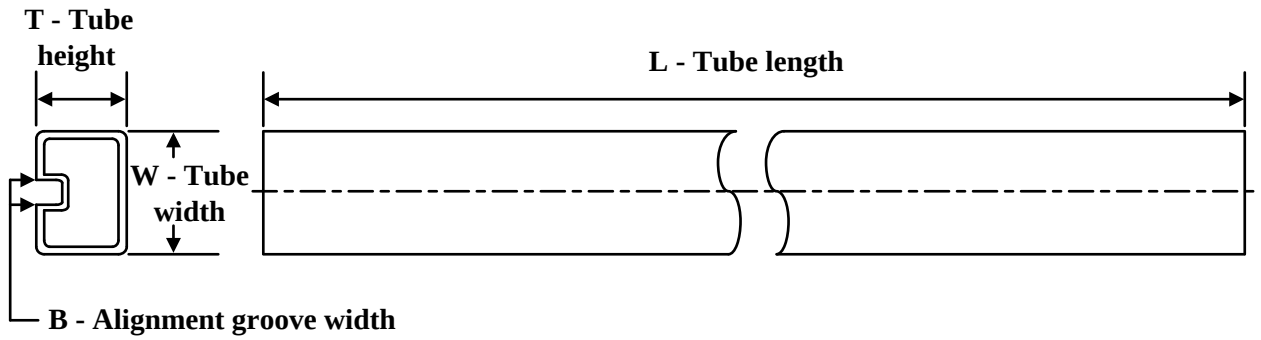
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC555CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC555CDR	SOIC	D	8	2500	356.0	356.0	35.0
TLC555CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC555CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC555IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC555IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLC555QDR	SOIC	D	8	2500	356.0	356.0	35.0
TLC555QDR	SOIC	D	8	2500	350.0	350.0	43.0
TLC555QDRG4	SOIC	D	8	2500	356.0	356.0	35.0
TLC555QDRG4	SOIC	D	8	2500	350.0	350.0	43.0
TLC555QDRG4	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

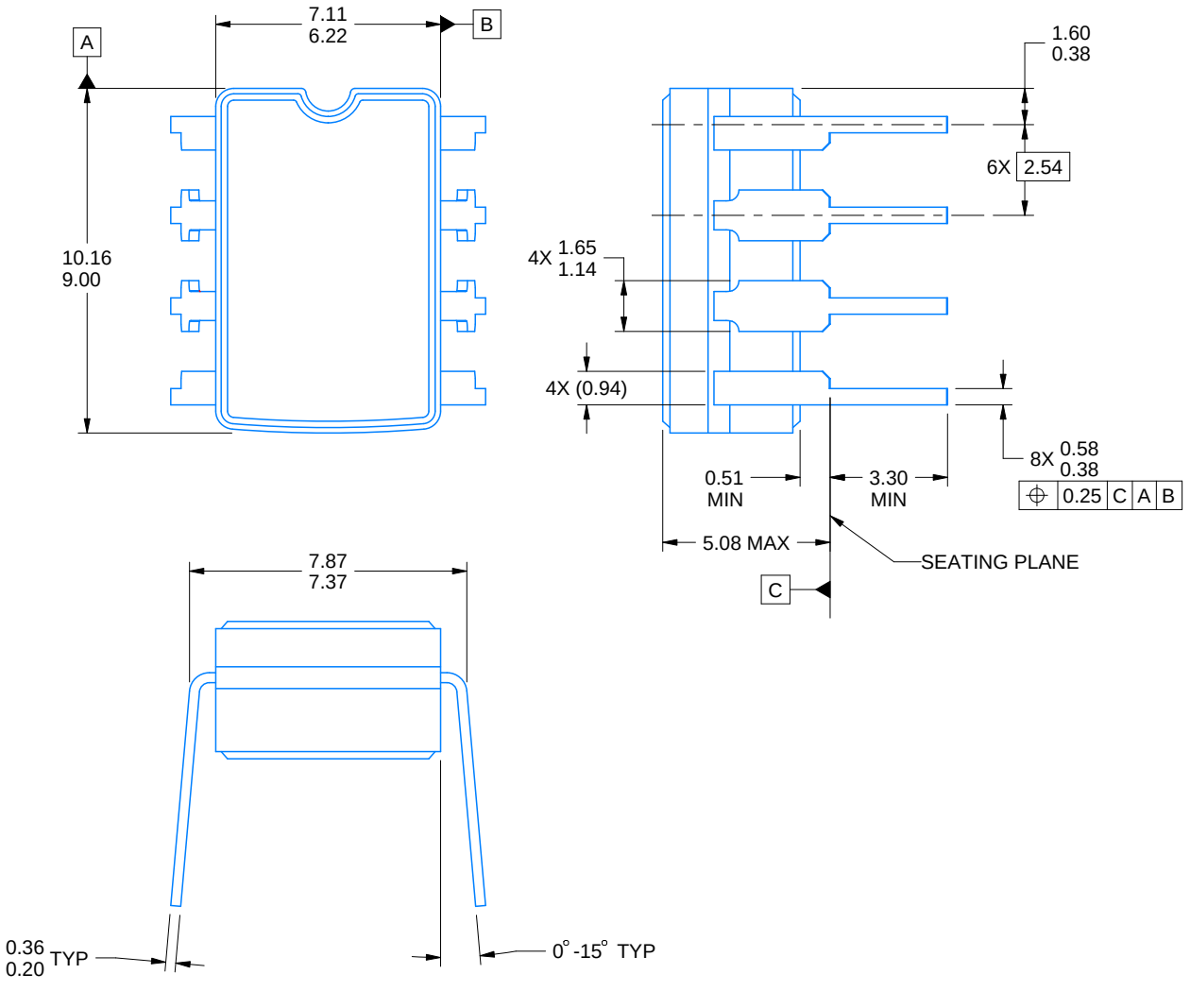
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-89503012A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC555CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC555CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC555CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC555CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC555CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC555CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC555CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC555CPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC555IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC555IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC555IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC555IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC555MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC555MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

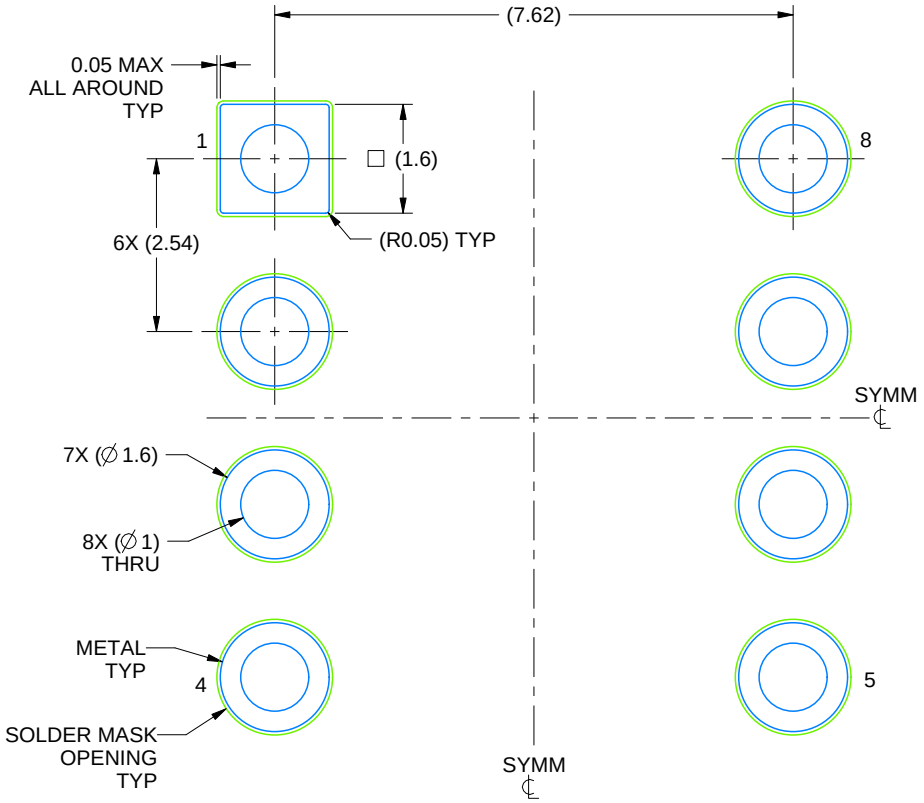
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

GENERIC PACKAGE VIEW

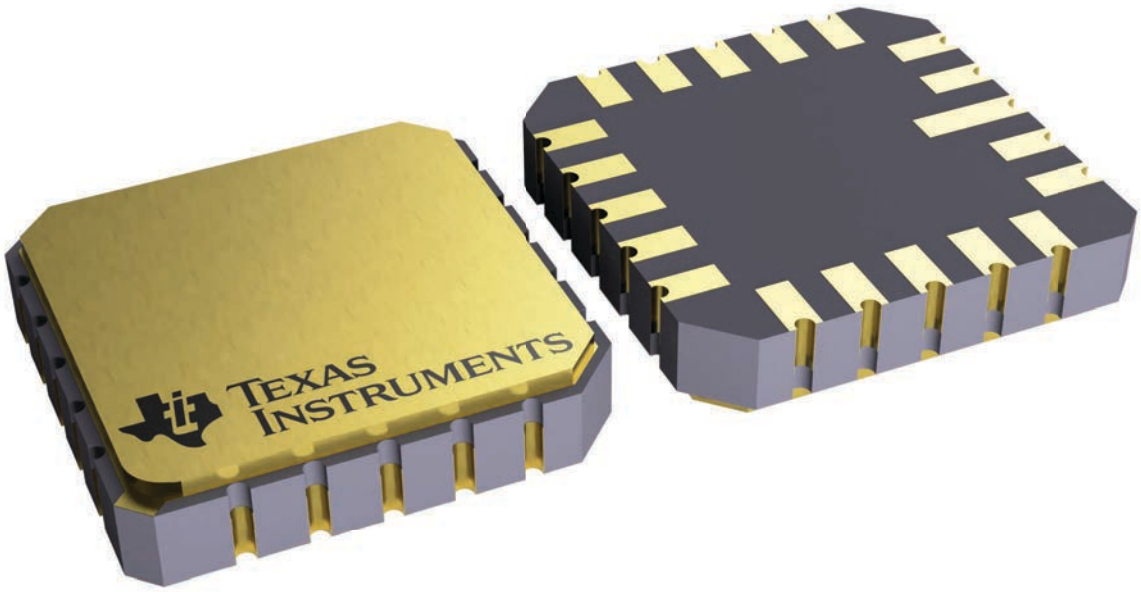
FK 20

LCCC - 2.03 mm max height

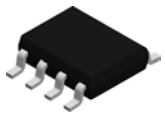
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

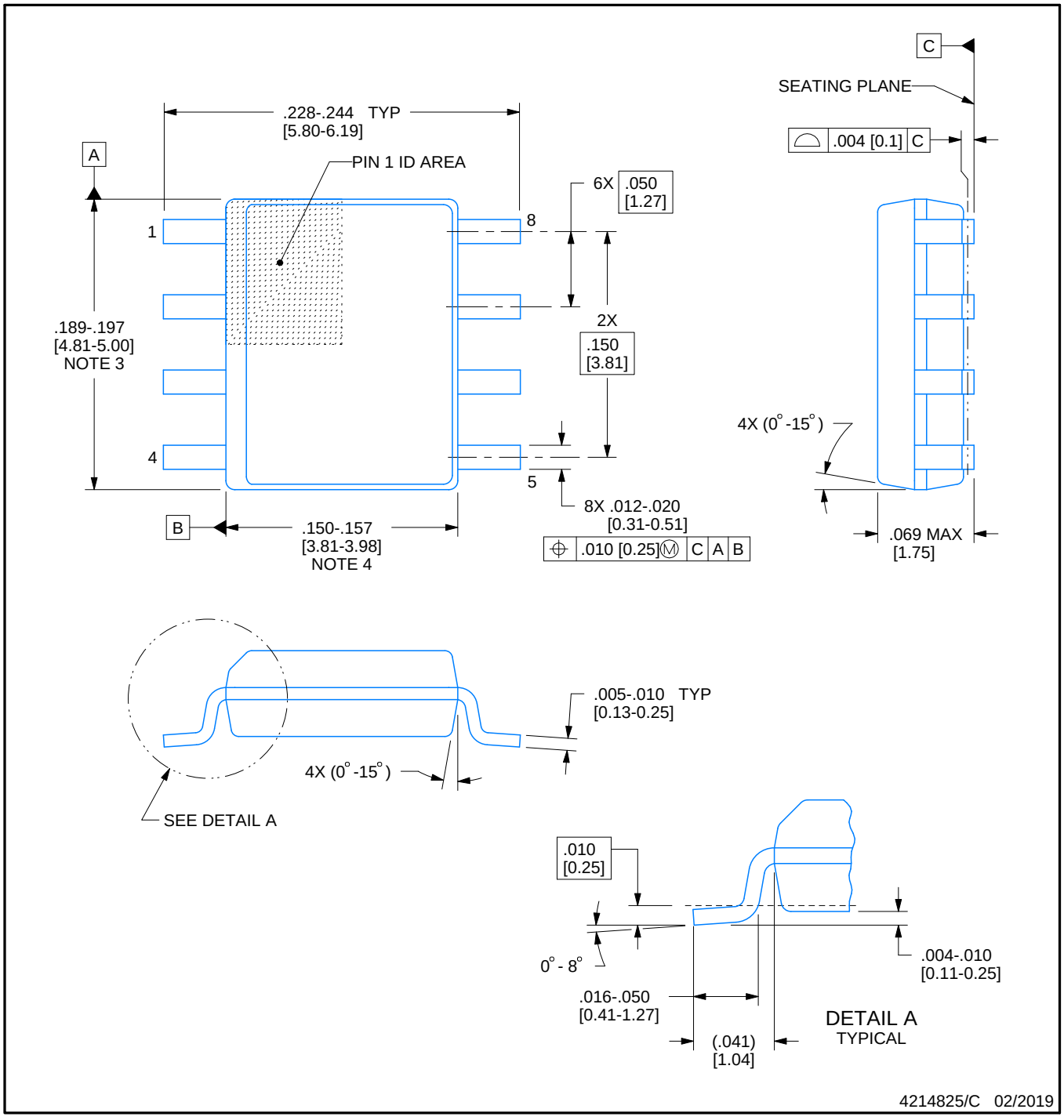


PACKAGE OUTLINE

D0008A

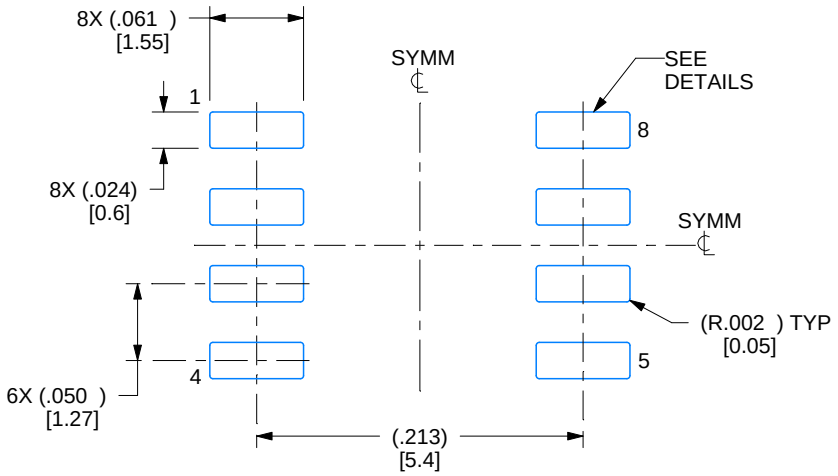
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

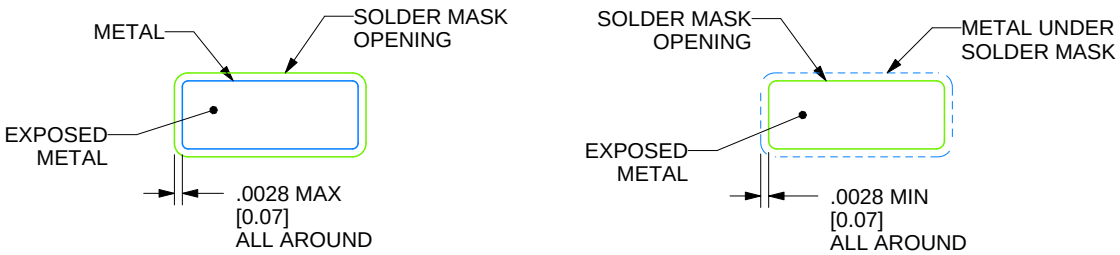


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

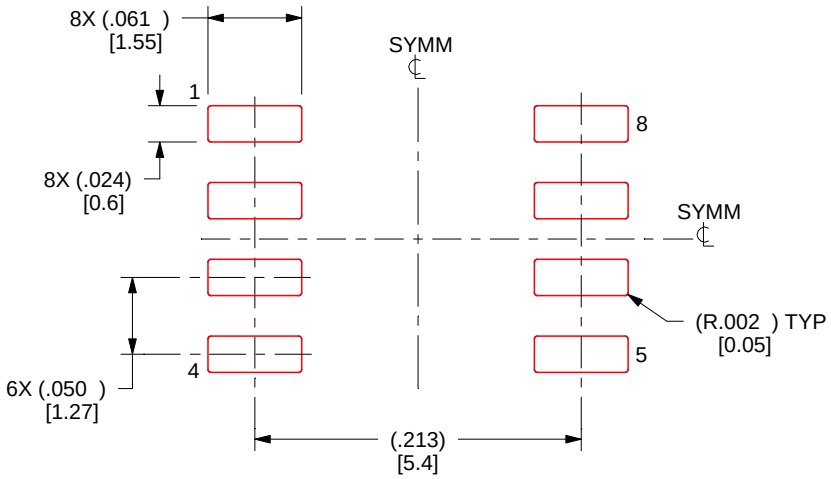
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

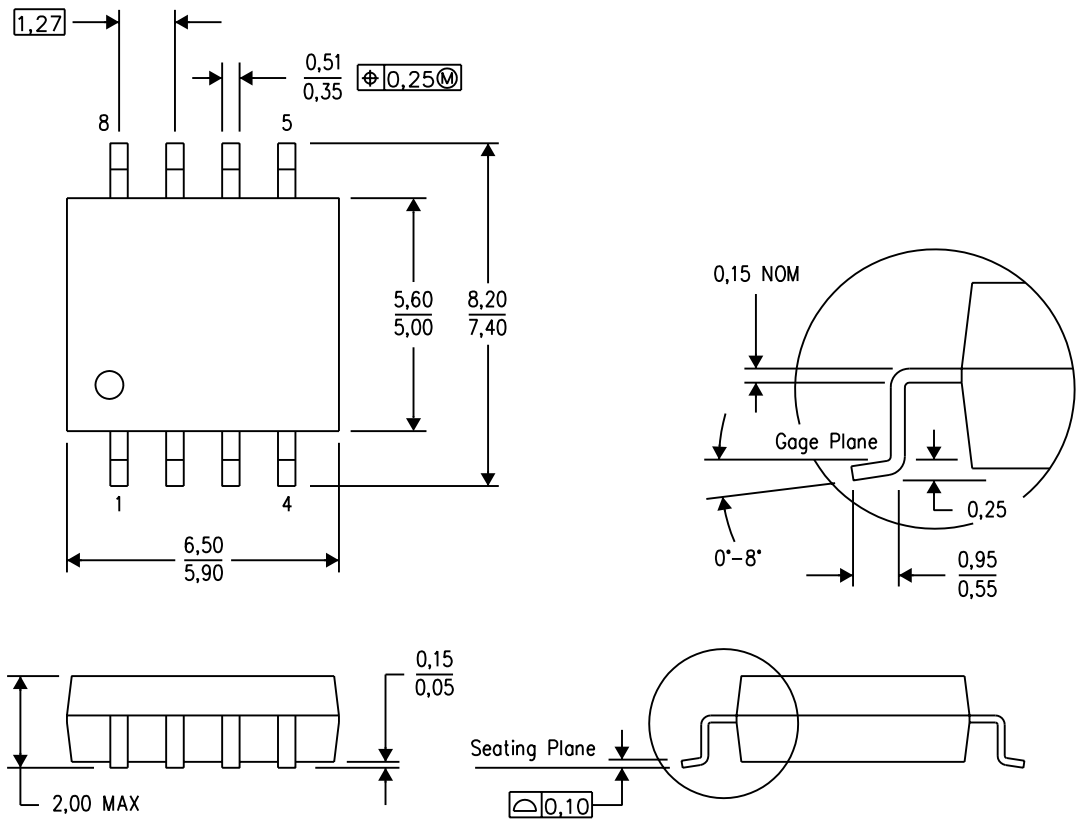
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

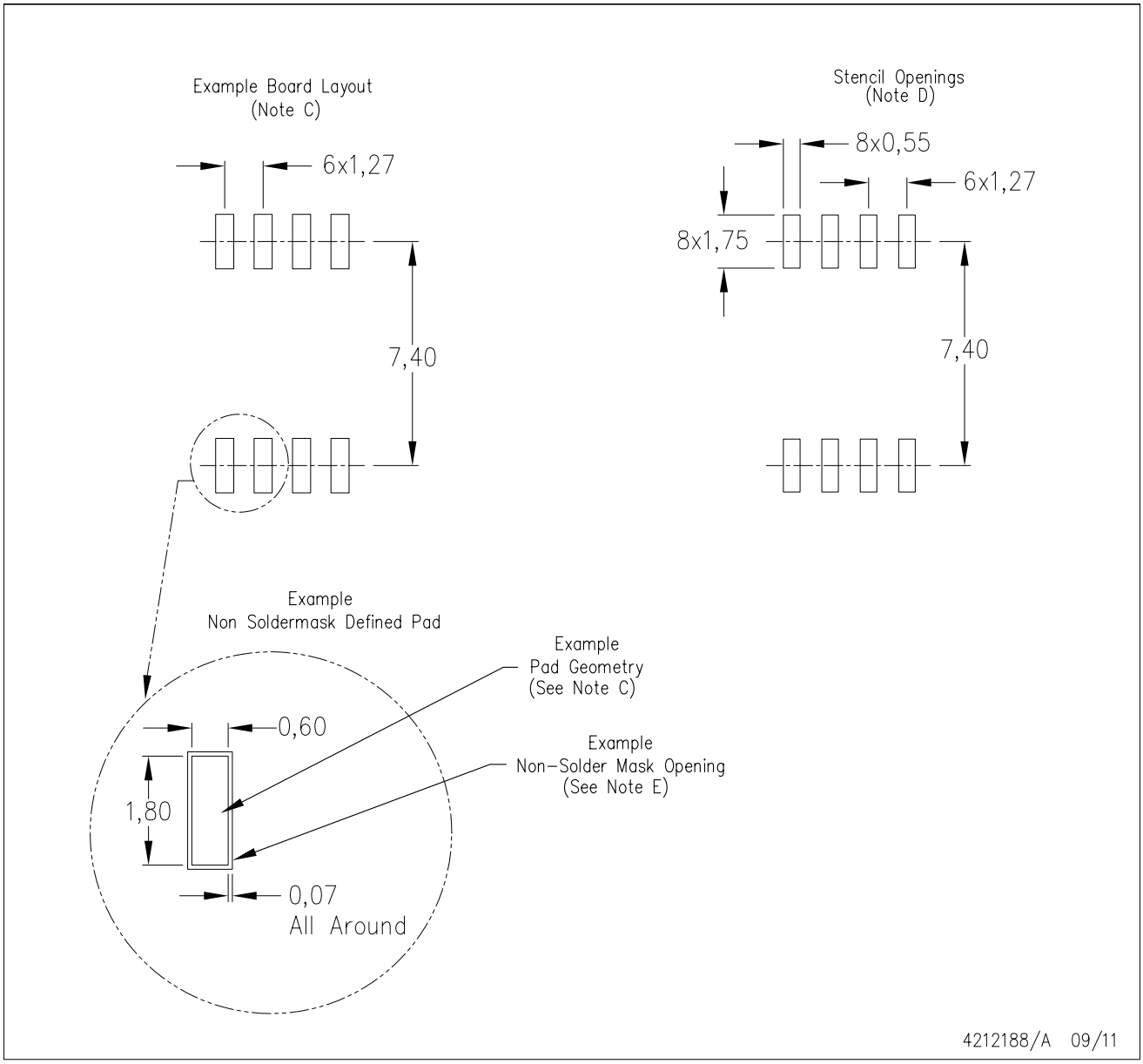
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

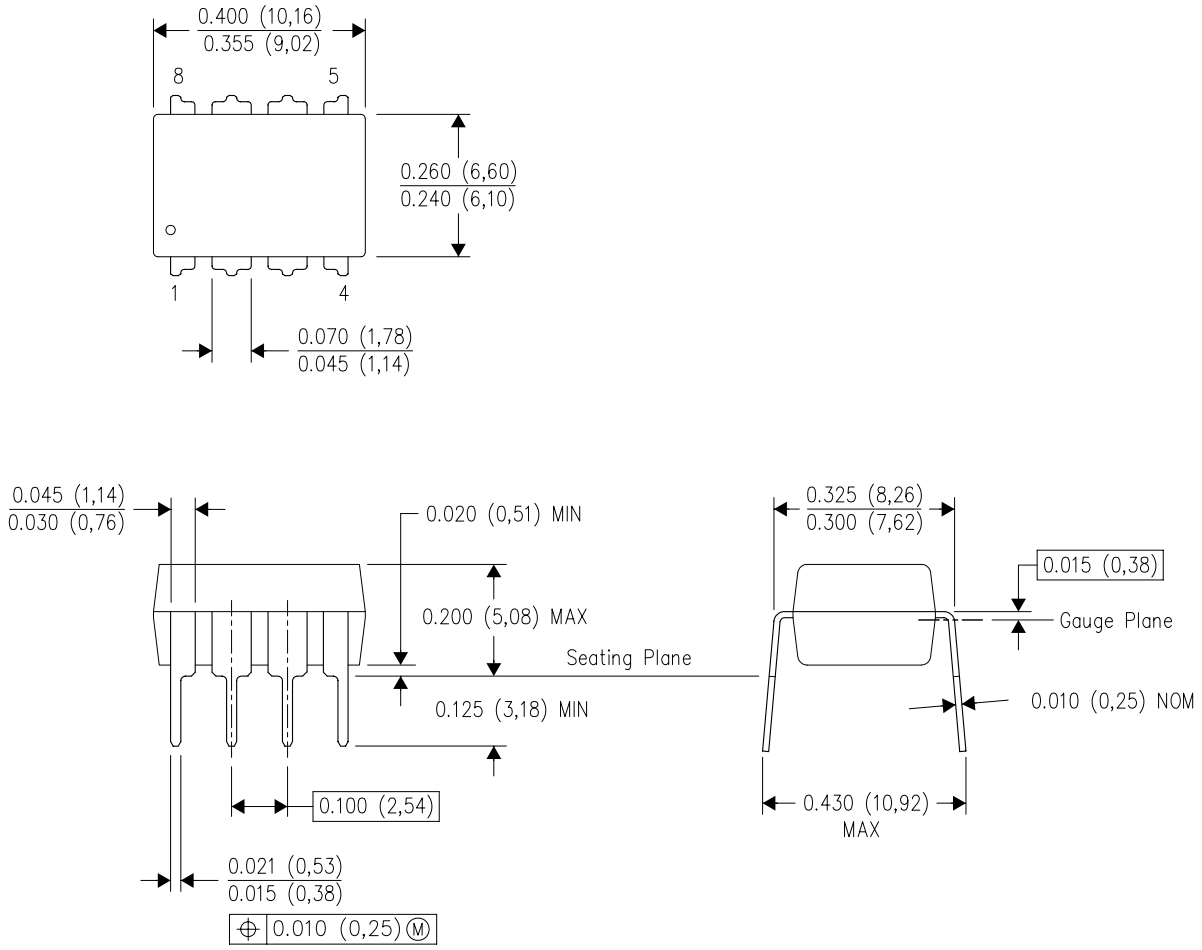
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



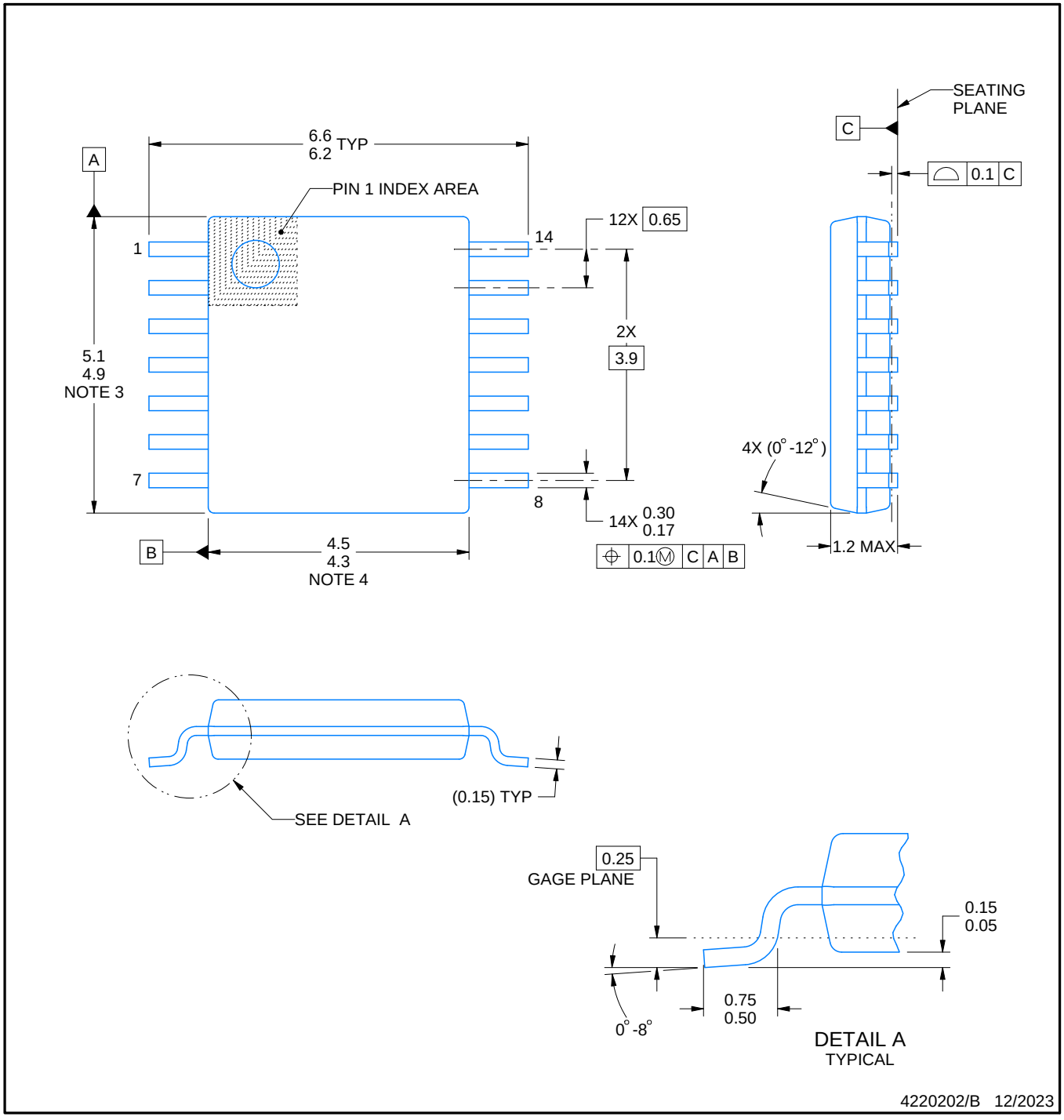
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0014A

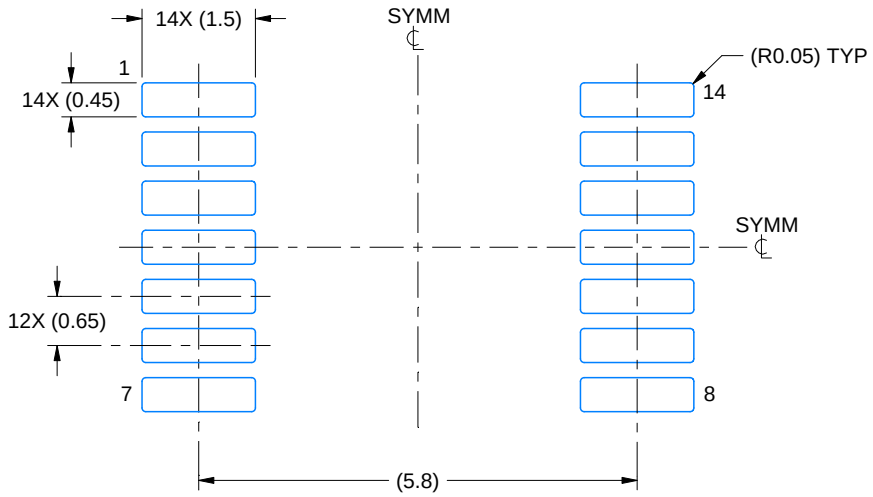
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

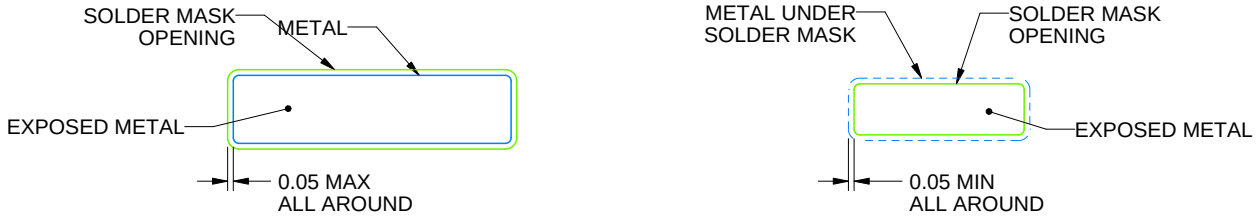


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

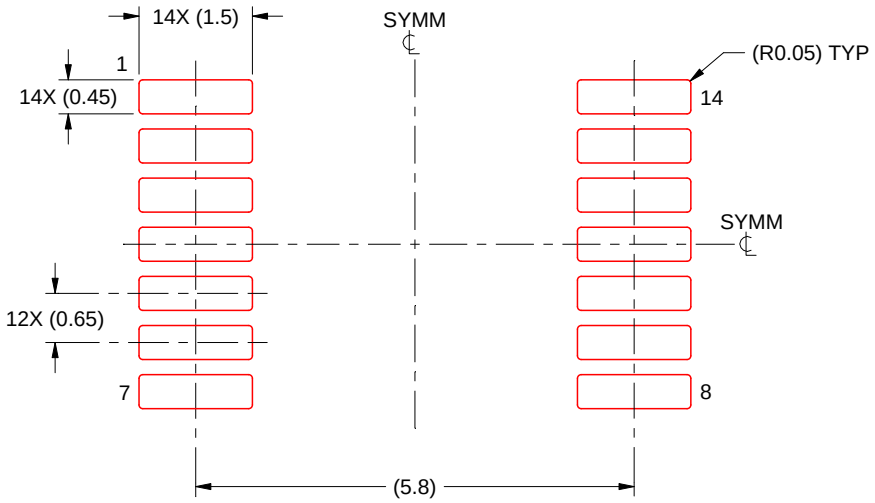


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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